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The OverMOS Project

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Abstract

The OverMOS project aims to create a fast radiation hard tracking detector sensor, based on High Resistivity CMOS technology. In a first prototype submission, different pixel and charge collection node geometries have been produced, which have lately been returned from fabrication and are currently under test.

Keywords: Tracking detectors, CMOS Active Pixel Sensor

1. Introduction

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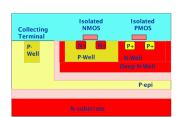
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CMOS technology has lately been introduced into particle 26 physics as a new technology delivering good quality radia-27 tion hard sensors at lower cost than conventional silicon sen- 28 sors. This is particularly relevant on the scale of future particle 29 physics projects at the large hadron collider, dealing with sili-30 con surface areas on the scale of hundreds of square meters.

Within the OverMOS design project, we are aiming to deliver 32 a CMOS active pixel sensor, where charge collection happens in 33 a fully depleted epitaxial silicon layer, rather than in a partially 34 depleted substrate. Using a CMOS imaging process (TowerJazz 35 180 nm) we are collecting charge deposited in a thin epitaxial 36 layer. Using a low doped epitaxial layer, we believe that full 37 depletion can be achieved, even at low bias voltages, allowing 38 to collect all deposited charge through drift. Amplification of 39 the charge happens in active electronics, embedded into deep 40 wells.



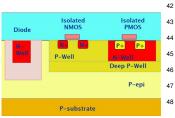


Figure 1: Depletion regions developing in P-epi on P-substrate and N-substrate. 49

Shown in Figure 1 is a cut view of the depletion developing for chosen layouts in P-epi on N-substrate and P-epi on P- 52 substrates. In either case the collecting well acquires all the charge deposited within the epitaxial layer. Our goal is to pro-54 vide a structure that can collect 90% of the deposited charge within <20 ns.

2. Test Structures

In a first approach we have submitted of order 30 test structures for both, P-epi on N-substrate as well as P-epi on Psubstrate, allowing us to look at charge collection for electrons as well as holes. Given an engineering run in TowerJazz 180nm technology, we have requested different resistivities and thicknesses for the epitaxial layers, in order to evaluate charge collection speed and depletion depth after irradiation for different biases.

The active test structures all contain a 5x5 matrix of pixel elements, differing in form-factor and electrode layout. Each of the inner 3x3 sensitive elements comes with an amplifier and shaper integrated into its deep central well, whilst the outer ring is used to bias the sensor and therefore make the inner cells behave as if within an infinite grid. This should allow to test these cells with realistic charges as given by minimum ionising particles.

Passive test structures have been embedded into both designs to allow for laser charge collection tests, as well as TCT measurements. A particular version of these structures sits on the side of the samples, supporting edge TCT to understand the vertical depletion profile.

In addition to these, a passive test structure designed by CERN has been submitted, allowing to check transistors as well as passive components before and after irradiation.

2.1. The Pixel Cell

The Layout strategy followed was to keep things simple: an existing amplifier used in the PImMS [1] project was adapted to sit inside the OverMOS pixel cell. The amplifier is placed inside an isolating deep well, and only connected to the charge collecting epi through P- or N- contacts (depending on the substrate).

For this initial test, we have submitted pixel cells (c.f figure 2) in different form factors, allowing more or less space within the deep well. Square form-factors (40x40 μ m) seem preferred when aiming at a pixel detector application, whilst elongated pixel cells (up to $40x800 \mu m$) are encouraged for a strip-like

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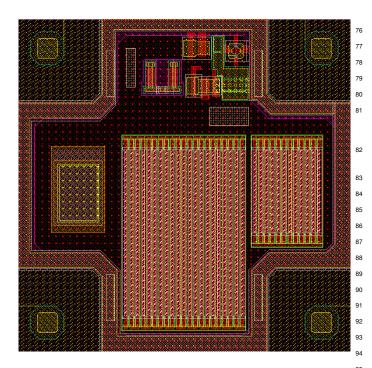


Figure 2: P on N example of the Pixel cell design, submitted in November 2014.

detector. We aim to understand the influence on signal timing, depending on where charge is deposited within a particular sen- 97 sor layout, allowing to maximise the usable space whilst keep- 98 ing the timing impact low.

3. Simulation

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TCAD simulation allowed us to evaluate the possible charge ¹⁰³ collection properties of these sensors before and after irradia-¹⁰⁴ tion: We have simulated both N- and P-substrate with the cor-¹⁰⁵ responding deep N- or P-wells for pixel embedded electron-¹⁰⁶ ics. We find that even for charges deposited underneath the ¹⁰⁷ deep well, the acquisition can happen within 20ns. A radiation ¹⁰⁸ model has been applied to predict performance after irradia-¹⁰⁹ tion. It shows that charge collection efficiency will be good up to $1 \cdot 10^{15}$ n_{eq} cm⁻², while it drops when simulating an order of magnitude more.

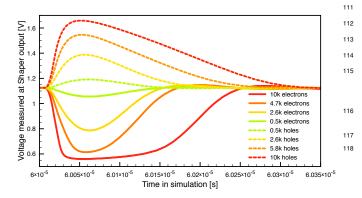


Figure 3: Amplification and timing performance of the embedded amplifiers for different simulated input charges.

In addition to the sensor behaviour, we have also run spice simulations of the pixel cell amplifier, allowing us to understand the expected timing performance of output signals (cf. Figure 3). The set of passive pixels submitted with the test circuits will allow us to judge on differences in performance due to either the bulk behaviour, or the amplifiers.

4. Test Plan

Tests are currently ongoing to measure a set of individual components, most of them transistors, irradiate them to different levels of ionising dose and measure them again. This should allow us to do a screening of components used in future designs, giving an indication of their behaviour with respect to dose.

Non-ionising effects will be observable in the sensor bulk, the epitaxial layer, by measurement of charge collection speed and efficiency in different regions. For this purpose, the test submissions contain passive arrays, that can be utilised for edge-TCT measurements, allowing to understand the depletion patterns in depth. The active arrays will be checked with laser injection, as well as radioactive sources to measure a response from known charge deposition.

5. Current Status and Conclusion

The first Wafers (5um, $20\text{-}30\,\Omega\,\text{cmP-epi}$ on P) have arrived early June and are currently being tested for electrical functionality, before further wafers with higher resistivity will be processed and delivered.

At the same time we already started to work on a larger scale chip that will hold many pixels of the same type, as well as discriminators, calibration mechanisms and a digital readout interface. This next submission is to show a functional larger scale chip with internal discrimination and understand whether the per pixel noise can be held low in a larger assembly. It will also allow to judge on the total timing performance of the chip and run the chip in a particle testbeam, where charge collection efficiency with different particle types can be verified.

Acknowledgments

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