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100 Mrad Radiation Tolerant CMOS Devices

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100 Mrad radiation tolerant CMOS devices

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Abstract

Test transistors and a complete mixed signal integrated circuit, fabricated in the Harris AVLSI-RA process, have been irradiated and shown to function well at total doses greater than 100 Mrad (1 MGy). Results are presented.

I. Introduction

Many applications for electronics with a high degree of radiation tolerance are becoming apparent in areas not well served by currently available technology. These applications tend to place a stringent total dose requirement on devices but have lower requirements for single event or dose rate tolerance.

The European nuclear power industry has many spent nuclear fuel reprocessing and fuel handling facilities. The need to operate efficiently in a commercial market and increasing statutory regulations are turning operators more and more towards remote handling techniques. Sensors, transducers, robotic arms, manipulators and remote viewing equipment are finding many uses within facilities into which man-access is impossible. A typical requirement for this equipment is a total dose, beta/gamma radiation tolerance of 100 Mrad (1 MGy), accumulated over a time period of between 2 and 25 years. (Absorbed doses are quoted in rad[Si] (Gy[Si]) throughout this paper.) Decommissioning and decontamination operations require a rather lower degree of tolerance, with 100 krad (1 kGy) usually being sufficient. International programmes to encourage the development of equipment possessing the necessary radiation tolerance for these applications exist [1] and some manufacturers do now offer suitable equipment [2 - 4]. However, these developments do not take full advantage of the capabilities of modern microelectronics because of the high total doses and the poor availability of radiation hardened components in Europe.

High energy physics experiments, in particular new accelerators, such as LHC at CERN, also have increasing radiation tolerance requirements. The total dose expected to be received by detector electronics in LHC is 10 Mrad (100 kGy) and 10^{14}neutrons/cm^2 over 10 years. Special electronics is being developed for detectors and very fast read-out circuits for these applications [5]. A number of processes are being examined as candidates for fabricating these devices, including the Harris, AVLSI-RA, bulk CMOS process. Some of the other processes are producing encouraging results but most remain in the laboratory or are not available on a wide basis [6]. Test transistors and real devices have been fabricated and radiation tested to determine their suitability for high total dose applications.

II. Overview of the Harris AVLSI-RA process.

The Harris AVLSI-RA process is a 1.2 micron bulk (epitaxial) CMOS process with two metal layers and a high value voltage independent precision capacitor. The process is very simple to design with needing no consideration to achieve radiation hardness. Harris specify 1Mrad (10kGy) radiation hardness and 10^{14}neutrons/cm^2. The process although guaranteed

only to these radiation levels seems to be much harder. This makes it very attractive for digital and mixed signal applications in radiation environments.

III. Experimental results and discussion

A. Gamma irradiation of Harris AVLSI-RA transistors.

Transistors fabricated on the Harris AVLSI-RA technology were irradiated using a cobalt-60 source. The transistors were irradiated biased with 5 volts and unbiased to 10Mrad (100kGy) at 55 rad/s (0.55Gy/s). The devices are grounded after irradiation and kept at room temperature. After 7 months the devices were heated to 120 ^{0}C for 14 hours and remeasured and then again stored at room temperature. The initial measurements were reported earlier [7]. Only a few devices were measured from one processing batch.

The biased 80:9 micron NMOS transistors after 10 Mrad (100kGy) show a very small reduction in gain and also a -400mv shift in threshold which anneals to around -300mv after 10 months. The sub threshold leakage current of these devices at 0 volts gate bias shows a three order of magnitude increase but they are still switched off sufficiently for operation in digital and most analogue applications.
The unbiased 80:9 micron NMOS transistors after 10 Mrad (100kGy) show a -200mv shift in threshold but a small reduction in gain. This then produced a shift in the characteristic of just more than -100mv at 200ua drain current. This then anneals slightly after 10 months to less than -100mv.
The biased 5600:1.5 micron PMOS transistors after 10 Mrad (100kGy) show no reduction in gain but a -200mv shift in threshold. There is no change in the characteristics after 10 months.
The unbiased 5600:1.5 micron PMOS transistors after 10 Mrad (100kGy) show a negligible reduction in gain. The measurements until 1 month after irradiation were taken with the drain at -5 volts. All other measurements were done with -2 volts. Correcting for this then gives approximately -100mv shift in threshold and no change in the characteristics after 10 months. These measurements are summarised for the PMOS on the annealing graph [fig 1].

B. Further Gamma irradiation of Harris AVLSI-RA transistors.

A different batch of devices was irradiated using a cobalt-60 cell at AEA Technology. The transistors were irradiated biased with 5 volts and unbiased. The doses used were 69Mrad (0.69MGy) at 217rad/s, 100Mrad (1.0MGy) and 125Mrad (1.25MGy) at 390 rad/s. The ambient temperature during irradiation was 20 ± 2^{0}C. Dosimetry was carried out with Red 4034 Perspex dosimeters and is accurate to better than 10%. The devices were grounded after irradiation and kept at room temperature. The first measurements were carried out during a three hour period after irradiation.
The biased 80:9 micron NMOS transistors after 69 Mrad and 125 Mrad (0.69 MGy and 1.25 MGy) show a very small reduction in gain and also a -400mv shift in threshold. The sub threshold leakage current of these devices at 0V gate bias shows a two order of magnitude increase but they are still switched off sufficiently for operation in digital and most analogue applications. Similar devices previously showed a -400mv threshold shift after 10 Mrad.
The unbiased 80:9 micron NMOS transistors after 69 Mrad and 125 Mrad (0.69 MGy and 1.25 MGy) show a negligible shift in threshold but a small reduction in gain. This then produced a shift in the characteristic of about -300mv at 1ma drain current. The sub threshold leakage current of these devices at 0 volts gate bias show very little change. Similar devices measured previously showed similar small threshold shifts after 10 Mrad.
The biased 5600:1.5 micron PMOS transistors after 69 Mrad, 100Mrad and 125 Mrad (0.69 MGy, 1.0MGy and 1.25 MGy) show a negligible reduction in gain but a -200mv shift in threshold [fig 2]. Similar devices previously showed the same threshold shift after 10 Mrad.
The unbiased 5600:1.5 micron PMOS transistors after 69 Mrad and 125 Mrad (0.69 MGy and 1.25 MGy) show a negligible reduction in gain but a -100mv shift in threshold. The sub threshold leakage current of the 125 Mrad device at low gate bias shows three orders of

magnitude increase which is not evident at 69 Mrad. It is not clear whether the difference is due to this particular device or the increased dose. This should not affect the device in most applications except possibly when used in long term switched capacitor storage switches. Similar devices measured previously showed the same threshold shift after 10 Mrad.

This is a very positive result and gives every indication that circuits built on this technology will operate successfully even after 100 Mrad (1MGy).

C. Neutron irradiation of Harris AVLSI-RA transistors.

Transistors fabricated on the Harris AVLSI-RA technology and which had previously been irradiated to 10Mrad (100 kGy) of gamma radiation were irradiated using the ISIS neutron source at RAL. The transistors were irradiated unbiased to 10^{14}n/cm^2 with 1Mev neutrons. The devices were grounded during and after irradiation and kept at room temperature.
None of the samples showed any appreciable change in their I/V characteristics. The noise of the unbiased 5600:1.5 micron PMOS device showed a 2 dB reduction in flicker noise. This may be due to the annealing of the damage caused by the gamma irradiation.
This is however a very good result showing a small effect on the flicker noise mechanism. The noise above the flicker noise corner frequency due to thermal noise is unaffected by either irradiation.

D. Gamma irradiation of Harris MX7-RH.

As well as the measurements on individual transistors it is important to confirm that a large system fabricated on the process will work after irradiation. RAL has built an MX7-RH chip for High Energy Physics applications which contains 128 low noise amplifiers, filters and an analogue output multiplexer. This 36 mm^2 mixed analogue and digital chip is used to accurately measure charge deposited by ionising radiation in silicon detectors. It has been extensively studied and instruments many thousand channels of electronics at CERN, Geneva.
Five MX7-RH fabricated on the Harris AVLSI-RA technology were irradiated using a cobalt-60 cell at AEA Technology. The transistors were irradiated biased with 5 volts to 100Mrad (1.0MGy) at 390 rad/s. The devices were grounded after irradiation and kept at room temperature. The first measurements were carried out during a twelve hour period after irradiation.
Within the first hour after irradiation two chips (4,5) were working but had a factor two increase in noise. The other chips had dead channels but the shift registers worked. Chip 1 had one third of the channels dead.
After 12 hours all channels worked on all chips. The noise and gain were slightly affected as shown in Table 1.

CHIP NUMBER	NOISE PRE-RAD mv RMS	NOISE 100MRad mv RMS	GAIN PRE-RAD	GAIN 100MRad
1	0.17	0.19	0.059	0.055
2	0.17	0.22	0.0525	0.0513
3	0.16	0.26	0.054	0.050
4	0.18	0.25	0.055	0.0525
5	0.14	0.17	0.050	0.0463

Table 1.

This is a very positive result and gives every indication that complete mixed analogue and digital systems can be built on this technology will operate successfully even after 100 Mrad (1MGy).

IV. Summary

Test transistors and MX7-RH integrated circuits, fabricated in the Harris AVLSI-RA process, have been radiation tested in a cobalt-60 environment to total doses of up to 100 Mrad (1.0 MGy) and, after short annealing, shown to exhibit relatively little degradation. This is believed to be the first time that results on this process at this level of total dose have been reported. The test data give very promising indications that devices can be built in this technology for in-cell remote operations and future hadron colliders at total doses of the order of 100 Mrad (1 MGy) and 10^{14}neutron/cm^2. Furthermore, this is a well supported commercial process.

V. References

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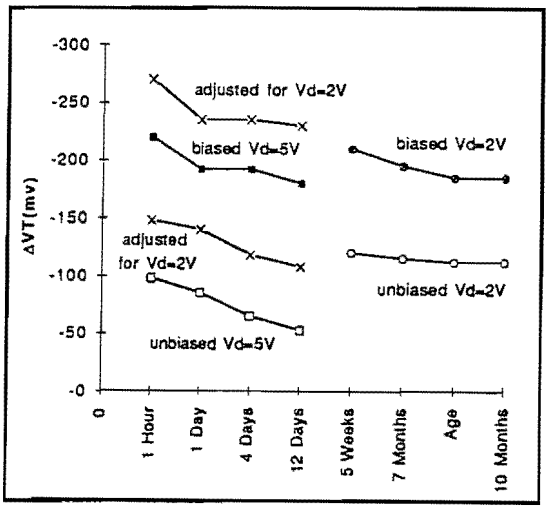

Fig 1. PMOS annealing after 10Mrad

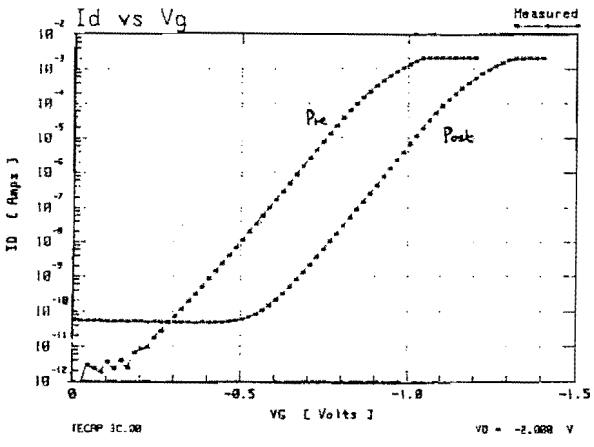

Fig 2.(Id vs Vg) PMOS after 100Mrad