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A 16 CHANNEL DMA CONTROLLER FOR THE PEP11 COMPUTER

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1. INTRODUCTION

This CAMAC unit controls Direct Memory Access (DMA) transfers between the main memory of a PDP11 computer and up to 16 CAMAC units. It works in conjunction with a type EC347A or type EC372 PDP11 crate controller. The DMA controller, crate controller and the units to be controlled are all located in the same CAMAC crate.

The intended area of application is to connect relatively slow data links such as modems or VDU interfaces into a computer system and the unit is intended to ease the task of programming such a system.

2. FUNCTIONAL SPECIFICATION

Each of the 16 CAMAC units to be controlled is allocated a channel number and has 4 associated registers. The channels are numbered 0 - 15 and will normally correspond with stations 1 - 16 in the CAMAC crate.

The unit is connected to the CAMAC highway and the PDP11 UNIBUS highway. Also a SYNC connection must be provided from each controlled unit to a multiway connector on the rear of the DMA controller; this may conveniently be done by using a CAMAC crate modified to have certain patch pins routed through to an extra station on the right.

The registers associated with a channel must be loaded before a valid transfer can take place, but may be overwritten or read at any time. The register contents are altered whenever a relevant transaction occurs.

The four registers for each channel contain

1. Word count - this is decremented at each transfer and hence contains the number of words still to be transferred. When this reaches zero an interrupt is raised.
2. Memory address - this is incremented at each transfer and contains the address in the PDP11 memory for the next transfer.
3. CAMAC NFA code - this holds the station number, function number and sub-address of the CAMAC unit involved in the transfer.
4. Status - bits in this control the mode of operation of the channel and record the state the transactions have reached.

These registers and also the channel number are selected by means of the Module Status Register (MSR). The lower byte of this contains the channel number and register number. The upper byte contains the number of the highest priority channel to have produced an interrupt.

The lower byte may be overwritten and read but the upper byte may only be read.

An Active Channel Register (ACR) contains the bit pattern representing the channels in which transfers are proceeding. This register may be read and selected bits are set or cleared by writing to the corresponding channel status register.

A LAM Register contains the bit pattern of channels with outstanding interrupts. This may be read. In addition, the number of the highest priority bit set in this register is encoded into the upper byte of the MSR.

In addition the LAM for the unit as a whole may be enabled, disabled or tested. A reset function is also available.

3. SUMMARY OF COMMANDS

The following is a list of valid commands

F(16)A(0) Write Channel Word and increment Module Status Register.

F(0)A(0) Read Channel Word and increment Module Status Register.

F(17)A(0) Set Module Status Register

F(1)A(0) Read Module Status Register

F(26)A(0) Enable Module LAM

F(24)A(0) Disable Module LAM

F(8)A(0) Test Module LAM Status

F(27)A(0) Test Module Status

F(1)A(12) Read Active Channel Register

F(1)A(14) Read Channel LAMs (bit pattern)

F(25)A(15) Reset Module

Z Clears all Registers and Initialises the Module.

The following CAMAC responses occur for the given conditions

X : is generated for all valid functions

Q : is generated if:

LAM is tested and LAM is set and enabled

or LAM status is tested and LAM is set :

3.1 F(17)A(0) and F(1)A(0)

The following is the allocation of bits in the Module Status Register (MSR) for an F(17)A(0) write or an F(1)A(0) read command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L		CL8	CL4	CL2	CL1	X2	X1			Ch8	Ch4	Ch2	Ch1	Cw2	Cw1

This register contains the channel word pointer and the LAM channel pointer. Bits 2 to 5 contain the channel address of the currently addressed channel, and bits 0 and 1 contain the word address within that channel of the word being accessed. Thus to read or write a channel word, the MSR must be set up to point to the word required, and then the operation carried out. However on reading or writing to

a channel word, the MSR is automatically incremented to allow the following word to be accessed without reference to the MSR.

The high byte of this register contains the encoded channel number of the highest priority interrupting channel, and has bits 8 and 9 patchable but preset both to 1's so that it can be read, and directly written to the low byte for ease of reaching the channel status word when an LAM occurs.

The highest priority is given to the leftmost module in a crate unless patching is done in a SYNC grader.

The most significant bit (of the high byte) indicates that the LAM is a valid one.

3.2 F(16)A(0) and F(0)A(0)

The allocation of the 4 channel words is as follows

Word Address		Channel Word
....00	CW0	Wordcount Register
....01	CW1	Memory Address Register
....10	CW2	NAF Register
....11	CSR	Channel Status Register

The channel words (CW0, CW1, CW2 and CSR) are accessed by means of the MSR, which is automatically incremented after each read or write operation.

The Registers are as follows

a) CW0 - Wordcount Register

This is a 16 bit register which holds the number of words remaining to be transferred.

b) CW1 - Memory Address Register

This is a 16 bit register which holds the memory location for the next word to be transferred.

c) CW2 - NFA Register

Only 14 of the 16 bits of this register are used and hold the codes for the CAMAC station, function and sub-address

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		N16	N8	N4	N2	N1	F16	F8	F4	F2	F1	A8	A4	A2	A1
		station					function					sub-address			

d) CSR - Channel Status Register

This is a 16 bit register with the following bit allocations

BIT

0 Enable Sync via front panel Lemo/P1.

1 Continuous transfer required.

2 Byte mode.

3 Enable Sync via appropriate B1 connector.

4 Enable End of Data (EOD) signal via appropriate B2 connector.

5 Enable EOD signal via front panel Lemo/P2.

6 Enable channel LAM.

7 End of Block (EOB) has occurred.

8 Not used.

9 Not used.

10 Not used.

11 Not used.

12 Not used.

13 Not used.

14 Time Out has occurred.

15 EOD has occurred.

When either of the Enable Sync bits are set, the channel is active, and the appropriate source (or sources) are enabled to start transfers.

B1 is the channel sync line in the rear Cannon connector.

B2 is the early termination line in the rear Cannon connector.

P1 is the dataway bus line P1 and the front panel SYNC socket.

P2 is the dataway bus line P2 and the front panel EOD socket.

The channel sync lines are wired individually to an external sorting device, and P1 and P2 are taken straight from the dataway. It is not possible to drive more than one channel with the same Sync pulse on P1.

The SYNC and EOD facility can be enabled to either or both of the channel EOD line in the rear Cannon connector and the front panel Lemo. The purpose of allowing Sync to be taken from P1 or P2 is so that it is possible to drive a single module without needing to take a connection to the rear Cannon connector.

The Enable Channel LAM bit allows the channel to generate a CAMAC LAM.

P1 has higher priority than any of B1 lines.

4. PHYSICAL LAYOUT

The DMA controller is a triple width CAMAC module. The front panel connections consist of two Unibus connectors (86 way Tekdata edge connectors), and three Lemo sockets, wired to dataway lines P1 and P2 and to the module's LAM.

At the rear there are two standard CAMAC highway connectors. A 35 pin Cannon connector brings the 16 B1 and the 16 B2 lines into the module. These lines are assigned to the channels on a 1 to 1 basis, and are connected to the appropriate sources elsewhere.

On the front panel there are a 16 bit display of the active channels and a 16 bit display of the going channels. The active channels are those in which a Sync bit is enabled, the going channels display flashed every time an actual autonomous transfer occurs on that channel.

5. DETAILED OPERATION

The unit is controlled by means of normal CAMAC operations. The registers are written to and read via the CAMAC dataway. A channel is activated as soon as its status word has had the appropriate bit(s) set; the wordcount, memory address and CAMAC codes must of course have been set up first.

Figure 1 is a block diagram of the overall unit.

Figure 2 shows the sequence of operations.

After initialisation, the sequencer stays in the wait condition (state 0) until a valid SYNC signal is received. When this occurs, a request-arbitration-grant sequence takes place to allow the DMA controller to become the UNIBUS master. A Non Processor Request signal (NPR) is generated and the sequencer then waits (state 2) until the Non-Processor-Grant signal (NPG) is received.NPG is acknowledged by generation of a System-Acknowledge signal (SACK) and the sequencer then waits (state 4) until the Bus-Busy signal (BBSY) disappears. When this occurs the sequencer generates its own BBSY and now has control of the UNIBUS with all other devices locked out.

At this time (state 5) the number of the channel with the highest priority valid SYNC is set in Memory-Address-Register 2 (see fig. 1).

This is the number of the channel over which the next word will be transferred by DMA.

If a higher priority SYNC has occurred in the time between

state 0 and state 5 of the sequencer then the higher priority channel will be chosen at state 5.

After state 5 any more SYNC signals occurring are ignored until the sequencer returns to state 0.

Next the wordcount for the selected channel is transferred via the Internal Data Bus (see fig. 1) to the Adder where it is decremented by 1 and the result saved temporarily in the Latches and then stored again.

The memory address is next transferred via the Internal Data Bus to the MEM Register and also to the Adder where it is incremented by 1 or 2 depending on whether an 8 bit byte or 16 bit word is to be transferred. The incremented address is saved temporarily in the Latches and then stored.

The CAMAC station, function and sub-address code is then transferred via the Internal Data Bus to the NFA Register.

Next the status word is transferred via the Internal Data Bus through the Adder to the Latches. Zero is added in the Adder so the Status word is not altered by this process.

The unit is now set up for a transfer to occur and in state 12 the direction of transfer is tested, and a CAMAC cycle interleaved with a UNIBUS data transfer takes place. This interleaving differs according to the direction of transfer. For transfer out of the PDP11 memory, the data must be available from the memory before S1 time in the CAMAC cycle (see fig. 4), whilst for data transferred into the PDP11 memory, the CAMAC cycle has to have reached S1 time to make the data available for writing into the PDP11 memory (see fig. 5).

During the data transfer any appropriate changes to bits in the status word will have been made, and at state 25 the updated status is

stored again. The CAMAC and UNIBUS cycles terminate and a test is made of whether continuous operation is set.

If continuous operation is required a jump to state 6 is made and the process repeats immediately without relinquishing control of the UNIBUS, otherwise a jump occurs to state 0 to wait for the next valid SYNC.

It is necessary for correct operation that the CAMAC data transfer operation should also clear the SYNC signal.

If any of the conditions zero-word-count, end-of-data or time-out has occurred, then the DMA controller will generate an interrupt signal. The number of the channel causing this interrupt may be read using the CAMMAC command F(1)A(0). This reads the current channel number in the lower byte and the interrupting channel number in the higher byte, so a simple byte interchange saves the current channel number and puts the interrupting channel number into the correct place for a CAMAC F(17)A(0) write command to select the interrupting channel. When this has been done, the status word may be read using F(0)A(0) to determine the reason for the interrupt.

6. SEQUENCE CONTROL

The operation of the unit is controlled by a microprogram (fig. 3) held in Read-only-Memory (ROM).

The microprogram word is 40 bits wide and horizontal coding is used except for one three bit field. (In horizontal coding each bit has a single function).

The timing and sequencing of the microprogram is controlled by a free-running oscillator driving a synchronous 5 bit scaler which is either incremented or loaded with a new value at each clock cycle.

A single-step facility is also provided for commissioning and maintenance purposes.

The microprogram word is split into fields (see fig. 6) with the following functions.

Field A — Sequencing control. Bit 1 determines whether a test with possible branching will be made and bits 2 to 4 select which of 8 possible tests will be made. These 3 bits are the exception to horizontal coding.

Field B — The address to which a branch will occur when a test specified in field A has a valid outcome.

Field C — Generates signals for UNIBUS control.

Field D — Generates signals for CAMAC control.

Field E — Generates control signals for the internal operation of the unit. Not all of field E is used, and there may be some redundancy.

The complete program is shown in fig. 3.

7. CIRCUIT DIAGRAMS

Circuit diagrams of the module are available as Daresbury Laboratory Drawings No. DL 01/9700 to DL 01/9710 inclusive.

FIGURE CAPTIONS

Fig. 1. Block diagram of the overall unit.

Fig. 2. Sequence of operation flow chart.

Fig. 3. Microprogram.

Fig. 4. Timing diagram and flow chart for CAMAC write cycle.

Fig. 5. Timing diagram and flow chart for CAMAC read cycle.

Fig. 6. Allocation of fields in the microprogram word.

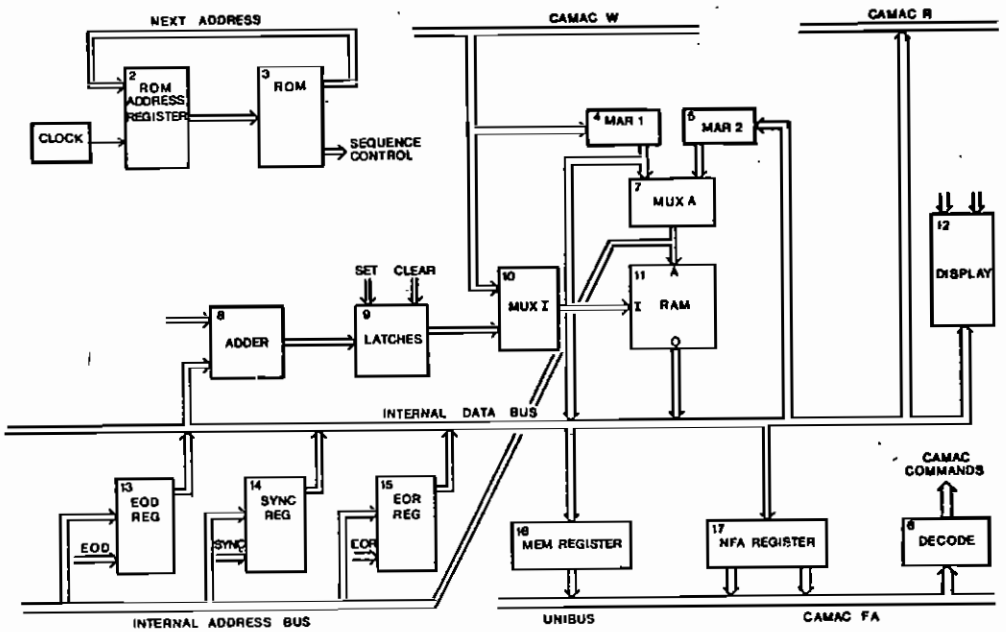

Fig. 1

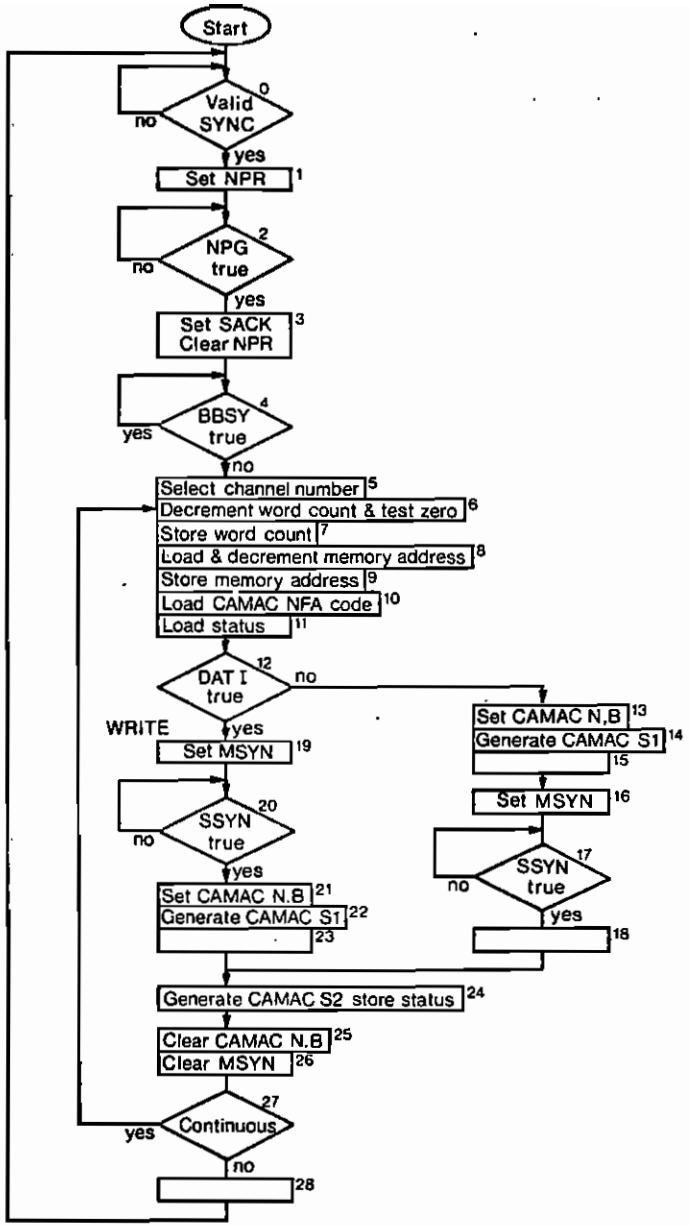
Start
0
Valid SYNC
no
yes
Set NPR 1
2
NPG true
no
yes
Set SACK Clear NPR 3
4
BBSY true
yes
no
Select channel number 5
Decrement word count & test zero 6
Store word count 7
Load & decrement memory address 8
Store memory address 9
Load CAMAC NFA code 10
Load status 11
12
DAT I true
no
yes
WRITE
Set MSYN 19
20
SSYN true
no
yes
Set CAMAC N,B 21
Generate CAMAC S1 22
23
Set CAMAC N,B 13
Generate CAMAC S1 14
15
Set MSYN 16
17
SSYN true
no
yes
18
Generate CAMAC S2 store status 24
Clear CAMAC N,B 25
Clear MSYN 26
27
Continuous
yes
no
28

Fig. 2

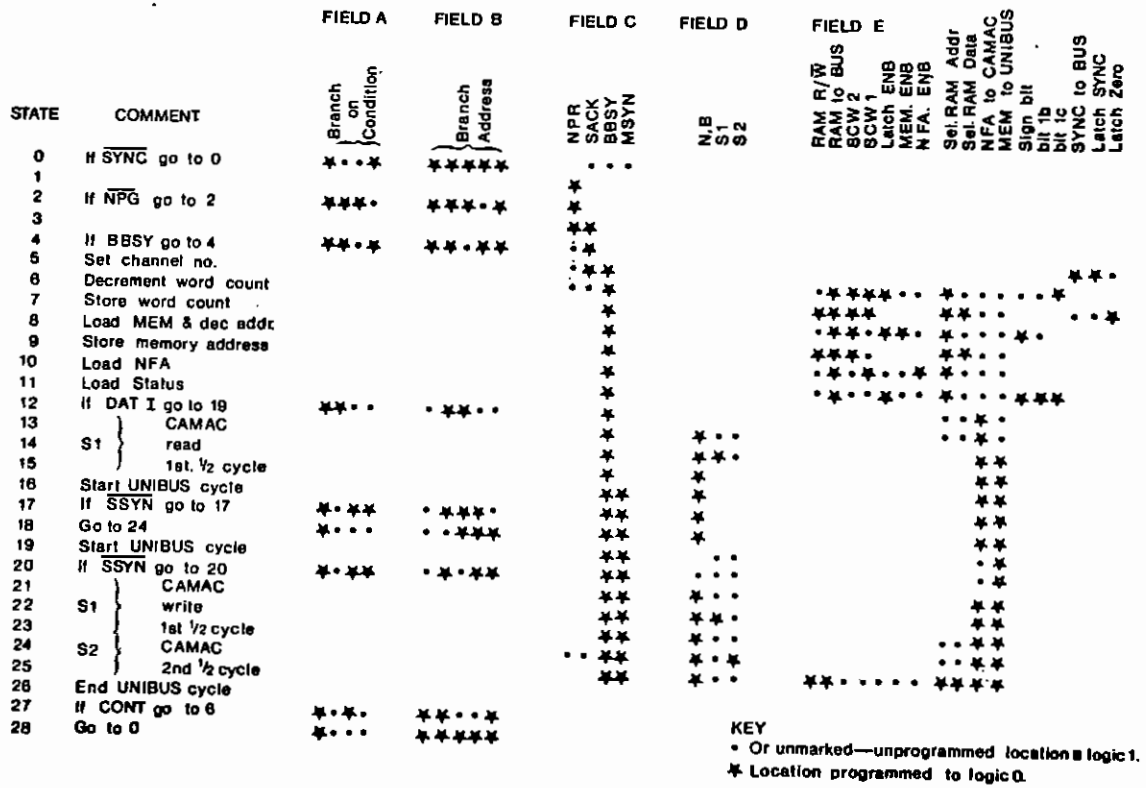
STATE
COMMENT
FIELD A
Branch on Condition
FIELD B
Branch Address
FIELD C
NPR
SACK
BBSY
MSYN
FIELD D
N,B
S1
S2
FIELD E
RAM R/W̄
RAM to BUS
SCW 2
SCW 1
Latch ENB
MEM. ENB
N FA. ENB
Sel. RAM Addr
Sel. RAM Data
NFA to CAMAC
MEM to UNIBUS
Sign bit
bit 1b
bit 1c
SYNC to BUS
Latch SYNC
Latch Zero
0 If SYNC go to 0
1
2 If NPG go to 2
3
4 If BBSY go to 4
5 Set channel no.
6 Decrement word count
7 Store word count
8 Load MEM & dec addr
9 Store memory address
10 Load NFA
11 Load Status
12 If DAT I go to 19
13 CAMAC
14 S1 read
15 1st. ½ cycle
16 Start UNIBUS cycle
17 If SSYN go to 17
18 Go to 24
19 Start UNIBUS cycle
20 If SSYN go to 20
21 CAMAC
22 S1 write
23 1st ½ cycle
24 S2 CAMAC
25 2nd ½ cycle
26 End UNIBUS cycle
27 If CONT go to 6
28 Go to 0
KEY
• Or unmarked—unprogrammed location = logic 1.
* Location programmed to logic 0.

Fig. 3

CAMAC Write ■ UNIBUS DAT I cycle

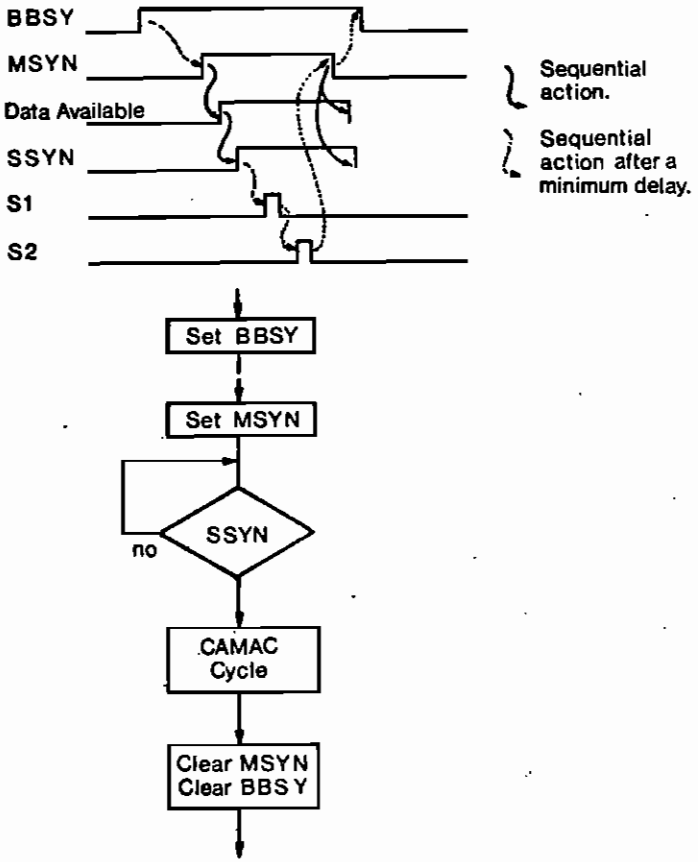

Fig.4

CAMAC Read ■ UNIBUS DAT O cycle

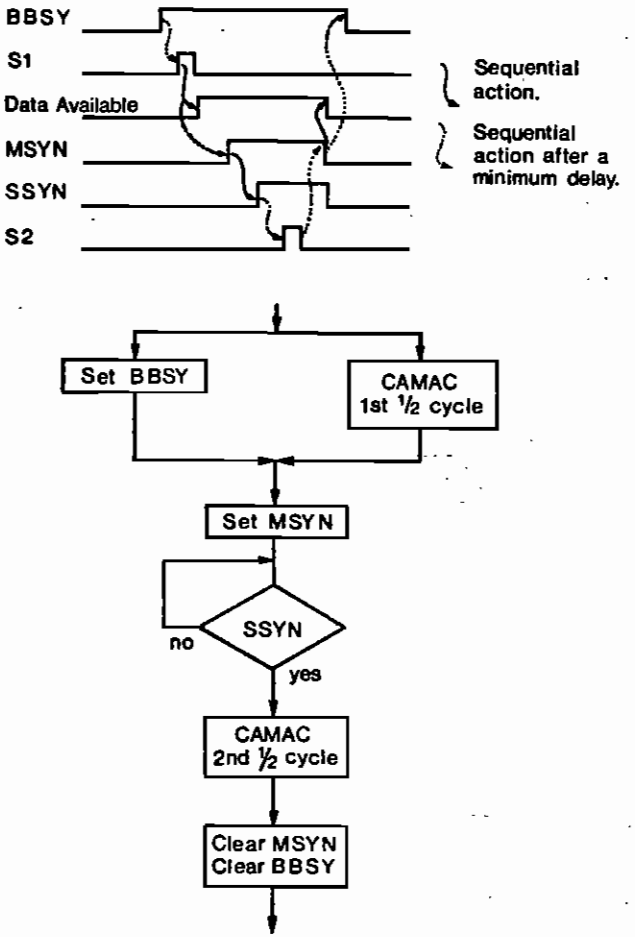

Fig. 5

Fig. 6