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AN INTRODUCTION TO LOGIC DESIGN USING GATE-ARRAYS

by

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1. INTRODUCTION

Application Specific Integrated Circuits, ASICs, are increasing in electronic function capacity and decreasing in production costs. ASICs are becoming a viable solution to design requirements, even in low volume production work.

A particular group of ASICs are gate-arrays. This document is aimed at introducing the electronics design engineer to these devices and their use.

2. GATE-ARRAY DESCRIPTION

In its basic concept the gate-array is an array of unconnected electronic logic elements. These logic elements or gates can be formed via various semiconductor manufacturing processes, complementary metal oxide semiconductor, (CMOS), and emitter coupled logic, (ECL), being the most common. The silicon on which a single array is manufactured is referred to as a die.

In the initial manufacturing process a matrix of dice is produced on a wafer of silicon, this matrix is produced by a set of lithographic and diffusion processes giving identical dice which at this stage remain in an uncommitted state. This means that all dice of a particular gate-array type are identical and all have no functional structure. The dice are a common source of transistor structures from which to create logic functions. The dice can be mass produced in the uncommitted state and customized for a particular function at a later stage. For this reason gate-arrays are known as semicustom devices. Mass production capability at this initial stage of manufacture is essential in giving a low cost technology.

The process of creating the electronic functional structure within the gate-array comes with the laying down of interconnecting metal layers on top of the uncommitted silicon structures within the array. The uncommitted transistor structures, known as cells, are given their functionality by this so-called metalization process. Metalization, usually with aluminium,

allows the creation of logic gates from the cells and also allows interconnections between gates to be made.

The use of the area within the array is divided in association with the use of the metal interconnects. Three different dedicated sections exist within the internal structure of the gate-array. One section contains the transistor structures for the construction of logic gates. The second section is the area between the structures where interconnections are made to join the logic together (routing). These areas are called routing channels.

A third section exists on the periphery of the die where the connections to the outside world are made; output driver cells and bonding pads are located here.

To keep the costs of manufacture down computer-generated placement of logic and routing of the interconnects between logic is carried out wherever possible. There are two common gate-array architectures which use a single layer of metal to create logic cells and interconnects; these are shown in fig.1. A single layer of metal is preferable as the deposition of one metal layer requires only one mask to be made thus minimising the cost of the finished i.c. The regular grid on to which logic cells are fixed allows the computer-aided production of the layout of the metalization mask to be performed more easily.

In fig.1 the routing of the logic interconnects in the "row-cell" case can be seen to be more constrained than the "block-cell" case. One dimension is blocked off by the strips containing the logic cell structures forming "x-axis" routing channels. The "row cell" case is more common and certain designs are accommodated more easily into this structure, when considering routing. A long serial logic path would fit more easily into this type of structure whereas a complex net of interconnects in a large random logic layout could have problems in being implemented.

The first consideration when designing a circuit within a gate-array is the number of cells available for use; this will vary with the functional complexity of the design. A totally regular design may use over 80% of the available cell structures without any routing problems. A random logic design, however, will have a lower cell utilisation density to allow routing and thus may be limited to the use of 60% or less of the array cells.

Normally the layout of logic within the array is left to the algorithms of an autoplacement and routing suite of software, but with a structured design approach the circuit can be tailored to maximise the probability of a successful implementation.

3. AN ARRAY IN DETAIL

The following describes the 70000 series of gate-arrays available through the Micro Circuit Engineering Falcon Scheme.

The purpose of the Falcon Scheme is to allow the evaluation of a small number of prototype parts of a design prior to large volume manufacture. This scheme also allows a low price route to small volume production, ideal for many laboratory applications.

Falcon software is mounted on an IBM PC and allows a schematic capture and simulation of the design created. It allows full operation and timing verification to be carried out and takes into account variances in the silicon batches used in manufacture. The software does not take into account any timing variations due to the layout of the circuit as no layout is carried out by the designer. The lack of a post-layout simulation at this stage is of minor importance for the majority of designs. Delays introduced by layout are usually small compared with a gate delay.

The minimum cost entry to the Falcon Scheme allows manufactured parts to be sent to the designer in an untested state. A "bomb-site" structure is provided by the manufacturer. The operation of the logic contained in the "bomb site" is tested to show that the manufacturing processes have been successful.

The technology used on this array series is 5 μm CMOS, i.e. complementary MOS with a minimum feature size on the silicon of 5 μm, the metal tracks and smallest transistor structures on the array being 5μm wide.

The software package used to design the Falcon Scheme gate-arrays is called BX[1].

A standard cell concept has been adopted in the use of BX. On the silicon a number of transistors are grouped together in what is known as a basic logic cell. There are enough transistors to make a two-input NAND or NOR gate within this cell. It is this size of gate that is referred to when expressing the size of a gate-array. When a more complex gate is required several of these basic logic cells are connected together. This grouping of basic logic cells and the interconnection of them is referred to as a standard cell. A standard cell may contain many basic logic cells.

The use of standard cells lends itself to the creation of libraries of interconection data on how to form cells from basic logic cell elements. This library concept is strictly adhered to with BX and a library of logic elements is used at the schematic capture level. A library part can be called up and placed as a logic element on a circuit diagram created in the schematic capture mode.

Only library parts can be used in the creation of a design, although modules can be made up from library parts and these modules in turn added to the library. This use of groups of library parts in modules can be used to create a structured design. The hierarchy created can be used in the automatic layout procedure. This allows functionally associated cells to be physically grouped together on the silicon if they are connected within a single module. Many critical timing areas can be dealt with in this way.

The interconnects between library parts are also inserted in the schematic capture mode. When the schematic data is translated into placement information the library part translates as a standard cell with all the basic logic cell interconnect data.

The basic logic cell is shown in fig.2. The example shows the basic logic cell configured as a NAND gate in terms of the field effect transistors and the layout required to bring about the required connections.

The use of standard cells allows the timing of a particular logic component to be standardised. All standard cells of a particular component are identical, using identical transistors and interconnection patterns. The timing may change between batches of silicon, however, which must be borne in mind, although this will be a global variation on the whole silicon die.

It is this characterisation of cell timing which allows circuits to be simulated in software. The time characteristics and function of each logic element in a design can be introduced in a simulator and the operation of the design verified. It must be realised that no account for delays due to tortuous routing can be introduced to the simulator in this software suite. This constraint means that highly critical timing paths which could lead to race conditions must be avoided.

It is possible to route tracks through polycrystalline silicon, known as poly. The router may use this option in its attempts to provide an interconnect, unless this is prohibited by prior arrangement with the manufacturer. These poly routes are resistive in comparison with a purely metal route and can cause more delay to a signal than was originally foreseen. This is because the R-C time constant for the connection including a poly route is higher due to the increased resistance. The poly routing tracks are embedded into the gate-array at the mass production stage and are accessed by metal tracks laid down in customisation. The use of poly in this way provides a more flexible routing system by allowing underpasses through logic areas to achieve interconnections.

4. DESIGNING BY USING GATE-ARRAYS

Technical reasons for using a gate-array.

1. Decrease in design time.
The time from the conception of a design to production of silicon is short in comparison with small-scale integration techniques. The use of simulators abolishes the need for hardware breadboarding.

2. Saving of board space.
The use of a gate-array in building a circuit will liberate printed circuit board area for other functions by design space minimisation. This may result in a single board design where a multi-board design is the standard solution.

3. Creation of a generalised building block.
A general circuit block used on several designs will make use of a gate-array for saving on layout costs and board production.

4. Reliability.
The use of a gate-array will lessen the problem areas of sockets and soldered joints which would be high in number in a system using conventional i.c.s.

5. Maintenance.
A single i.c. replacement is required to rectify a problem in a complex area of circuitry. This will cut down man hours spent on maintenance and also number of spares held.

6. Cost.
All the above items can be used to decrease the cost of a design both in its implementation and operation.

When designing using a gate-array the parameters of the array must be studied in some depth. It may be necessary in the light of these parameters to change the original design concept. This is a valid part of the design process even if the design is to be a new implementation of an already verified design.

Generally a design loop is entered which is shown in fig.3. It may be necessary to circle this path several times before a final design is decided upon.

Several points need consideration before commitment to a design.

1. Will the design partition into blocks that can fit easily into an array?
   If the overall design is too large for a single gate-array it may be necessary to split up the design. The logic then placed within the gate-array must be viewed with the aim of maximising the gate-array usage.

2. After partitioning what will the pin count be on the final device?
   The partitioning of a design is usually obtained at the boundaries of logic functionality. This method of partitioning will usually minimise the number of pins to integrate the gate-array with the rest of the circuit. Consideration of the connections to the outside world must always be given at this early stage as only a limited number of device package types are available.

3. Will the chosen array allow the realisation of the design speed?
   The speed of the silicon used in an array should be viewed as the slowest speed that is possible from a batch. A design that will run over all speed considerations will run on all subsequent batches of silicon.

   It should also be noted that the speed operation must be considered at the pins of the device. It is possible to have the internal gates operating at speeds that are impossible to achieve at the output pins. This is due to the fact that the output driver cells with higher driving capability than the internal cells are substantially slower. A loading factor is also placed on the output cells, this may not be applicable to the real i.c.s working environment.

4. Where are the critical timing paths of the design?
   Timing critical paths must be identified and if the design can not be clock driven or staticised with latches then pins to external timing components must be provided. Delays formed by internal cells should not be used to delay signals as these are not consistent between silicon batches and may result in one batch of i.c.s working whereas another will not. This means that monostable action obtained as shown in fig.4 MUST NOT be included.

5. Will the design be routable? (approximately 60% of the gates can be used for a random logic design; 80% can be used for a regular structure of design).
   The complexity of the design must be considered at all times. A highly complex design has in effect less gates to be designd in. This is due to the fact that a lower density of gate utilisation must be used to allow for complex interconnects between logic elements to be routed.

6. Are there any areas of high "knitting factor" in the design?
   It should be noted that routing problems may be caused by only a few interconnects or a minimal amount of complex logic connections when routing. These lines or areas are highly knitted into the design and exhibit a high "knitting factor". Examples of this are clock lines and wide architecture logic (bringing together many signals from the design into one small area).

   A clock line may have to be split on to several input pins. Wide architecture logic, many logic functions spread through a design which then are combined, may have to be placed externally to the array and the signal lines brought out on pins. (Fig.5 shows an example of this.)

7. Can the i.c. be tested if it is built?
   It may be very difficult to test physically the completed i.c. as no access is given to the internal structure unless the designer allows for this by allocating pins as monitors or test drivers. An example of this would be a many-bit long ripple-through counter. To test this counter fully without a testing mode would take many clock periods and may be prohibitive in time usage.

5. SIMULATION

When a design has been entered via the schematic capture it is then necessary to simulate the behaviour of the circuit using the BX simulator. The design must be simulated until it fails and then the failure mechanism must be investigated. The failure may be an expected effect, for instance the design speed has been exceeded, but it may have been something unforeseen. The failure mode must be understood to give a good confidence level in the design operation.

A basic concept with simulation is to toggle all nodes of the circuit in the simulation and to verify the effect on the output pins. All variables in silicon speed and temperature must be simulated.

A high level of confidence in the designed operational performance can be obtained if the testing patterns are specified correctly by the designer.

IT MUST BE STRESSED THAT AN INTERNAL ERROR IN DESIGN, ONCE MANUFACTURED, CANNOT BE FIXED BY ADDITION OF RESISTORS, CAPACITORS OR LOGIC. INTERNAL MODIFICATIONS ARE NOT POSSIBLE WITHOUT THE PRODUCTION OF A NEW METALIZATION MASK.

6. THE REAL I.C.

When the design is complete and has been thoroughly simulated the design data is sent on a floppy disk to the manufacturer. At the beginning of a month all designs received are collected together to be manufactured. Wafer sharing is carried out to keep the cost as low as possible.

Thirty days later the i.c.s arrive back with the designer in an untested state. The designer must then test the i.c.s. The manufacturer is satisfied that the processes used in making the array have been successful by checking the function of a test structure placed on each array.

Typical results have shown that approximately 80% of the devices received will work perfectly.

The largest array used in the 5 μm CMOS process available is a 1440 gate equivalent array. The first design processed by Daresbury in this technology used 660 of these gates. The design exceeded its expected operating speed of 10 MHz and will run above 12 MHz on the silicon received in the initial batch.

7. CONCLUSIONS

Application Specific Integrated Circuits are a useful tool in circuit design.

A design can be implemented quickly using such a system as BX.

Errors can occur in design by adopting a superficial approach to using ASICs in design tasks.

A basic understanding of the technology is required to ensure that a design can be best fitted to the technology available.

The designer must also learn to iterate the design and to have flexibility in its realisation when using a gate-array.

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REFERENCES

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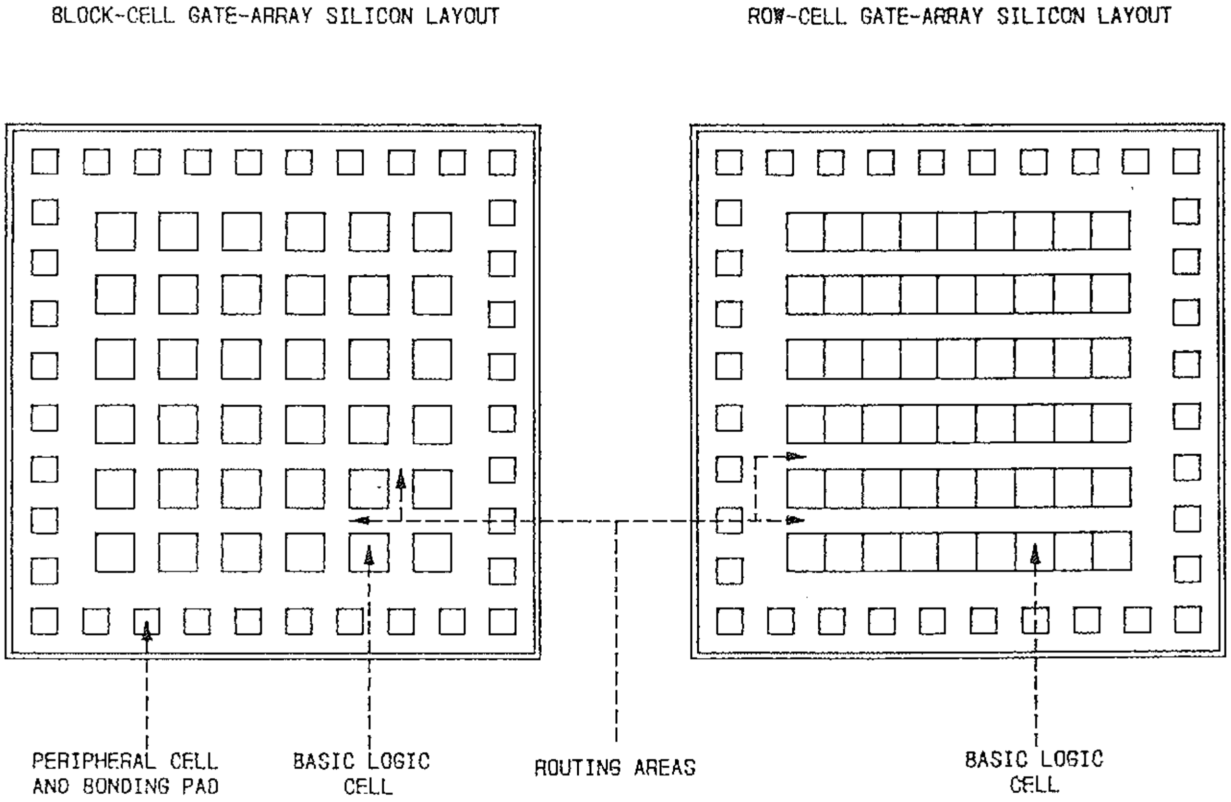
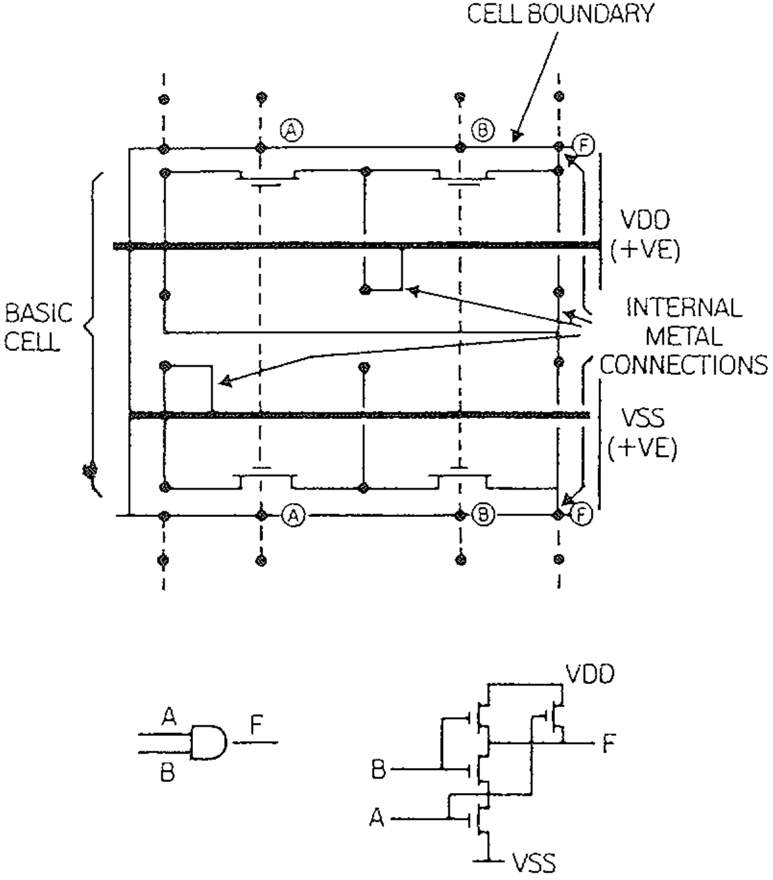

BLOCK-CELL GATE-ARRAY SILICON LAYOUT
ROW-CELL GATE-ARRAY SILICON LAYOUT
PERIPHERAL CELL AND BONDING PAD
BASIC LOGIC CELL
ROUTING AREAS
BASIC LOGIC CELL

Fig.1



(courtesy of MCE)

Fig. 2

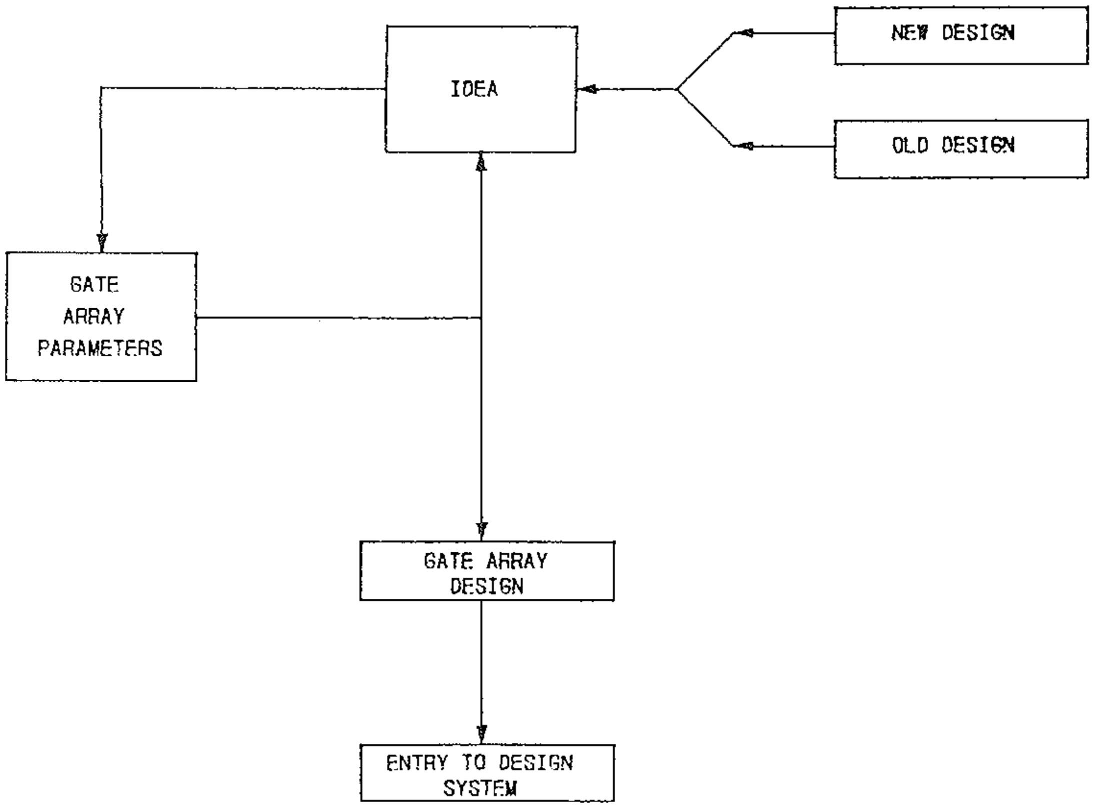
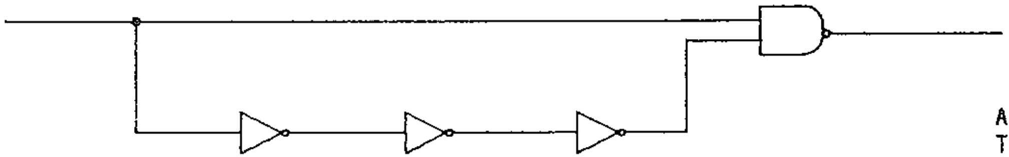
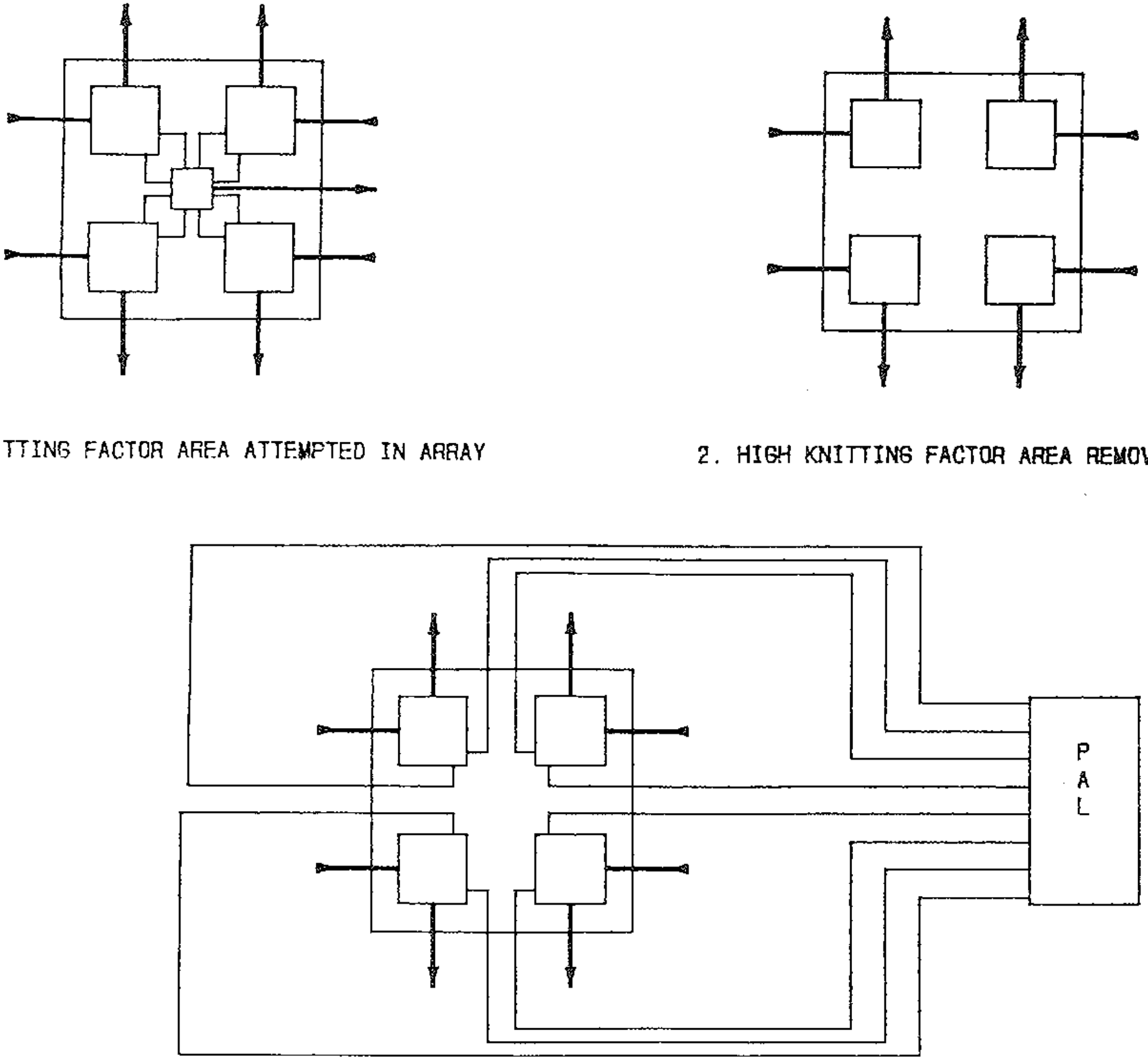

IDEA
NEW DESIGN
OLD DESIGN
GATE ARRAY PARAMETERS
GATE ARRAY DESIGN
ENTRY TO DESIGN SYSTEM

Fig. 3



A MONOSTABLE CONSTRUCTED THIS WAY IS NOT PREDICTABLE DUE TO VARIATIONS IN THE SPEED OF SILICON BETWEEN BATCHES.

Fig.4



1. HIGH KNITTING FACTOR AREA ATTEMPTED IN ARRAY

2. HIGH KNITTING FACTOR AREA REMOVED

3. REMAKE HIGH KNITTING FACTOR AREA EXTERNAL TO ARRAY

Fig.5