

# technical memorandum

Daresbury Laboratory

DL/CSE/TM42

## TEMPERATURE CONTROLLED ENVIRONMENTS FOR DIGITAL TO ANALOGUE CONVERSION

by

A. OATES, SERC Daresbury Laboratory.

OCTOBER, 1992

G92/226

Science and Engineering Research Council

DARESBUY LABORATORY

Daresbury, Warrington WA4 4AD

LENDING COPY

© SCIENCE AND ENGINEERING RESEARCH COUNCIL 1992

Enquiries about copyright and reproduction should be addressed to:—  
The Librarian, Daresbury Laboratory, Daresbury, Warrington,  
WA4 4AD.

ISSN 0144-5677

**IMPORTANT**

The SERC does not accept any responsibility for loss or damage arising from the use of information contained in any of its reports or in any communication about its tests or investigations

## TECHNICAL MEMORANDUM

### TEMPERATURE CONTROLLED ENVIRONMENTS FOR DIGITAL TO ANALOGUE CONVERSION

by

A. OATES

JUNE 1992

A61A

S.E.R.C

DARESBUY LABORATORY

DARESBUY

WARRINGTON

CHESHIRE

WA4 4AD

## SUMMARY

This study investigates techniques to achieve the best performance of a DAC and how to achieve repeatable stable results.

High resolution Digital to Analogue converters are investigated with the intention of using them for control and calibration applications requiring 16 bit resolution.

True 16 bit performance cannot be achieved without controlling the ambient temperature in which the devices operate.

## INTRODUCTION

The purpose of this study was to evaluate the performance of several high resolution Digital to Analogue Converters with the aim of producing a system capable of true 16bit performance over a wide operational temperature range.

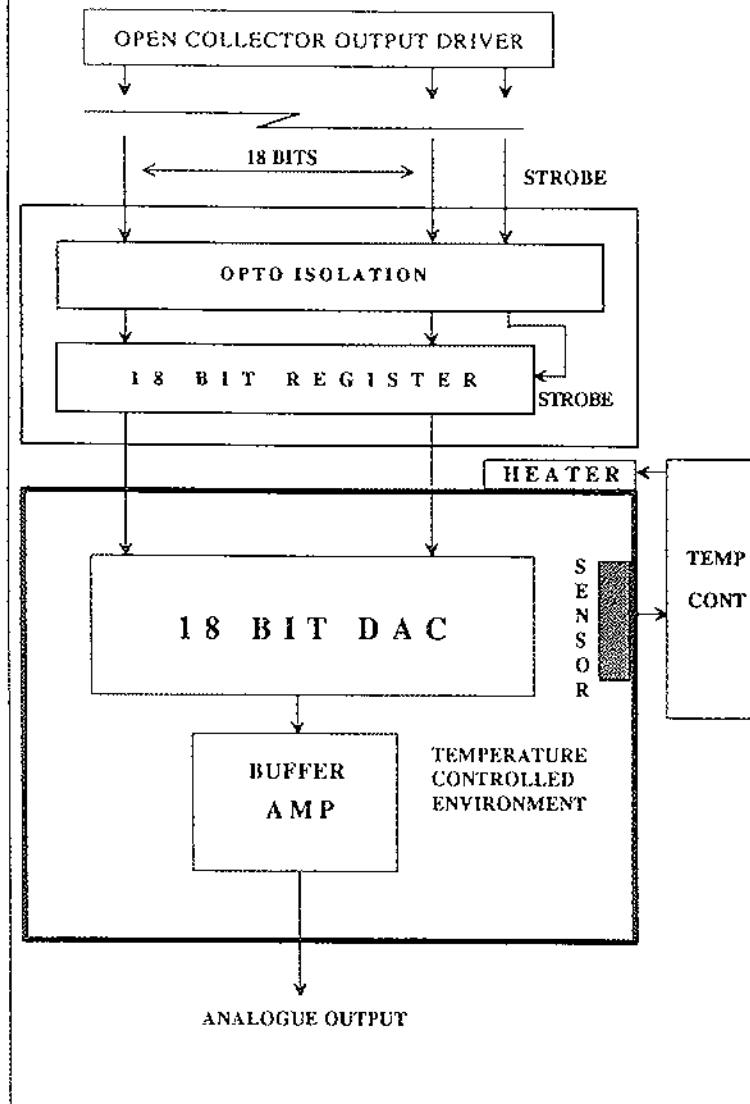
A self contained dual DAC unit was produced which incorporated several principles to improve overall performance.

1. An 18 bit converter was used to guarantee true 16 bit performance.
2. The DAC IC and all sensitive electronics were placed in a temperature controlled environment.
3. The digital input was isolated from the analogue electronics.
4. The DAC unit was designed to be placed where the analogue signal was required, not in a crate environment.

High precision DAC's are used regularly on calibration and control applications and recent requirements for automatic calibration techniques for Voltage to Frequency Converters and for highly stable power supply control references prompted the study.

**Figure 1**

Schematic of a DAC unit being driven from a digital output driver.



## DESIGN CONSIDERATIONS

### THE CHOICE OF DIGITAL TO ANALOGUE CONVERTER

The heart of the complete unit is the Burr Brown DAC729KH. This converter was chosen out of three devices evaluated as follows:-

Sipex SP9380-18

Analogue Devices AD1139K

Burr Brown DAC729KH

After evaluation of the technical data for the three devices it was found that any of the three 18 bit devices listed above could be used. Differences relevant to this application between the Burr Brown device and the two other devices are discussed below.

### ADVANTAGES OF THE DAC729KH

- 1) The DAC729KH was significantly lower cost compared with the others.
- 2) It was noted that both the other two devices had a non adjustable linearity and although originally exhibit 18 bit linearity they had a drift in parts per million per 1000 hours. In time the linearity could drift out of specification thus making the device un-serviceable. The DAC729KH would also drift but due to the adjustable linearity could be re-calibrated and so brought back into specification.

### DISADVANTAGE OF THE DAC729KH

The disadvantage with the Burr Brown device is that it needs more external components than the other two devices. These extra components adjust the linearity to the full 18 bits while the other devices should be 18 bit linear without adjustment.

Even with the cost of the extra components added the DAC729KH price was still the lowest cost device.

### CONCLUSION

It can be seen that the DAC729KH represented the best all round choice for the design. Being of lowest cost, and similar performance, and is likely to give the longest service of the three devices because of the ability to re-calibrate the linearity.

### SPECIFICATIONS FOR THE DAC729KH

#### TEMPERATURE DRIFT

From the DAC729KH data sheet

#### TEMPERATURE DRIFT

Gain drift typ = +/- 3ppm per degree Celsius

Offset drift typ = +/- 2ppm per degree Celsius

Reference typ = +/- 2ppm per degree Celsius

total +/- 7ppm per degree Celsius

16 bit accuracy requires  $(10^{**6} / 2^{**16})/2 = 7.63\text{ppm}$   
so the ambient temperature must be controlled to within

$$\frac{7.63}{7.00} = 1.09 \text{ degrees Celsius}$$

A temperature control tolerance of  $\pm 0.5$  degrees is therefore acceptable.

## LONG TERM DRIFT

From the DAC729KH data sheet. ( Ref 1 )

STABILITY LONG TERM	
Gain typ	$\pm 5 \text{ ppm/1000 hours}$
Offset typ	$\pm 5 \text{ ppm/1000 hours}$
reference typ	$\pm 5 \text{ ppm/1000 hours}$
-----	
worst case max	$\pm 15 \text{ ppm/1000 hours}$
-----	

It must be noted that the specification of 16 bit accuracy over 500 hours can be approximated from the above specifications.

## LINEARITY

From the DAC729KH data sheet ( Ref 1 )

Differential linearity error  $\pm 2 \text{ ppm / degree Celsius}$   
 Long term linearity error  $\pm 2 \text{ ppm / 1000 hours}$

$$\text{max error} \quad \frac{\pm 2 \text{ ppm}}{\pm 4 \text{ ppm}}$$

The DAC729KH is capable of 18 bit linearity. To reduce this to 16 bit would require a temperature change of.

$$\frac{7.63 - 2}{2.00} = 2.8 \text{ degrees Celsius}$$

Therefore the previous specification on page 14 for 1.09 degrees temperature control is the dominant factor.

**Note** - long term drift and temperature drift have been treated separately.

## ANALOGUE CONVERTER CIRCUIT

( figure 1 shows a overview of the DAC unit being driven from a digital output driver unit in a CAMAC crate. )

## RANGE CONFIGURATION

The DAC729KH produces a current output of 0 to -2mA this had to be converted to a voltage using an operational amplifier as a current to voltage converter for each range. Feedback was provided by four 5K ohm resistors internal to the DAC729KH.

An internal operational amplifier is also provided in the DAC IC. This was not used as the connection of the DAC IC to external equipment made the DAC IC susceptible to damage due to a fault in external equipment or by user error.

The op-amp chosen to perform the output driving was the PMI OP07. This device although inexpensive, has very low offset drift, large gain and good linearity and did not degrade the performance of the DAC within the limits of consideration.

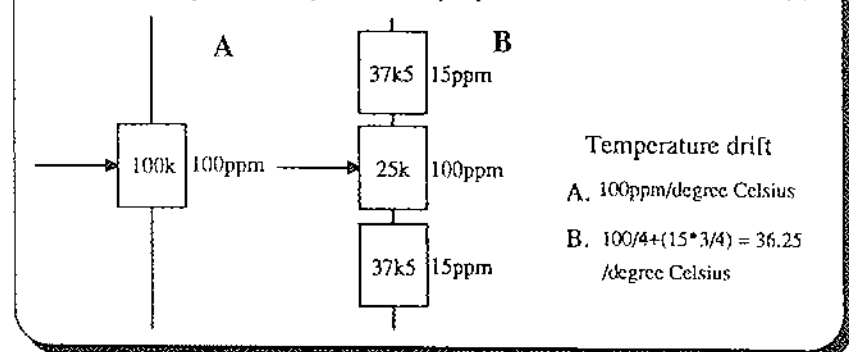
## OUTPUT VOLTAGE RANGE SELECTION

The Voltage range was selected by changed by changing a 16 pin DIL header on the analogue PCB.

The range selection resistors internal to the DAC are designed to be highly stable but these resistors would need to be matched to greater than 1 part in  $2^{**18}$  to permit no re-calibration of gain and offset after a range change. Thus the header used to change the ranges also connects in a different set of adjustment potentiometers for each range.

Each adjustment potentiometer has the provision for a series resistor at each end. These resistors if fitted can reduce the adjustment span therefore increasing the ease of calibration. This reduced the effect of instability in the potentiometer.

**FIGURE 2** Comparison of temperature stability of potentiometer and combination resistors

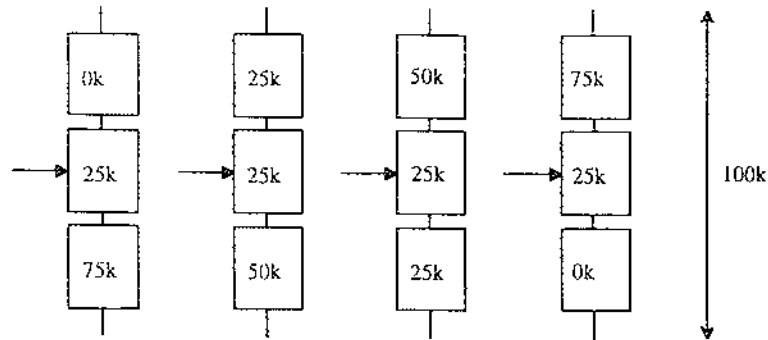


It must be noted that the above method has two major advantages.

1. Reducing the sensitivity of calibration adjustments therefore making calibration easier.
2. Increasing the units temperature stability, see figure 2.

Resistors had to be selected on test because the adjustment range may lie outside the middle quarter span covered by the potentiometer. Resistors were selected in one of the following configurations.

FIGURE 3. Gain resistor configurations



The technique shown in figure 3 was used for gain, offset and linearity adjustments. If the extra stability was not required the resistors could be replaced by links and the value of the potentiometer increased accordingly. This would result in a coarser adjustment. The same approach applied to the ability to change range without re-calibration if this was not required one set of gain and offset potentiometers would be sufficient for all ranges.

All components were specified to be the most stable parts which could be used within reasonable price and size limits. The majority of resistors used were 15ppm/degree Celsius temperature drift.

#### OVEN CONTROLLER CIRCUIT

The temperature controlled environment was provided by a die-cast box and was heated by power transistors. Transistors were in a linear control circuit which enabled the majority of the power consumed to be transferred to oven enclosure without using pulse width modulation commonly used with a resistive heating element. This was to eliminate any switching noise appearing on the analogue output due to high frequency components of power switching using a non continuous modulation.

#### INTERNAL POWER DISSIPATION

With the oven circuit off the power dissipation from the analogue circuit caused a thermally insulated oven enclosure to rise 10 degrees Celsius above ambient temperature ( the dual DAC circuit was calculated to dissipate approx 3 watts ). Therefore if an maximum ambient temperature of 35 degrees Celsius was reached the oven must run at 55 degrees plus a safety margin to maintain temperature control

#### SOLUTION USED

It was decided not to run the oven at greater than 45 degrees as higher temperatures produce a greater thermal shock to the components when the unit heats or cools from ambient temperature. The alternative to running at a higher temperature is to reduce the insulation thus allowing heat loss through convection. The extreme was used where the oven enclosure would not be insulated at all. With no thermal insulation there would be a problem with heat loss across the enclosure with the point farthest from the heating element running cooler due to convection losses. This was reduced by four heating elements one at each corner of the enclosure.

FIGURE 4. Transistors, Power controlled by Vc the control voltage

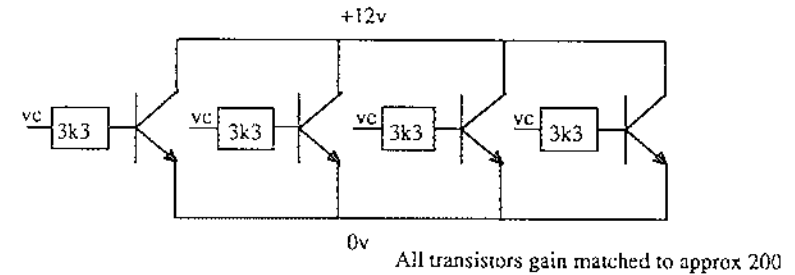
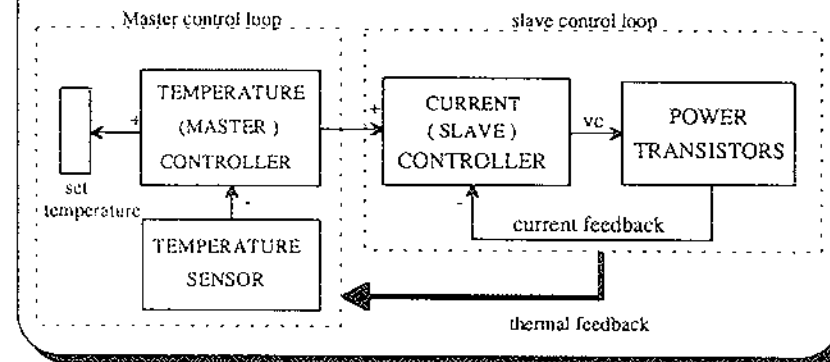


Figure 4. shows the transistors used. Four were used to overcome heat loss across the enclosure. One transistor being bolted onto each corner of the enclosure. The transistors must be gain matched or the temperature distribution will again be uneven across the enclosure. It can be noted that the power supplied by the controller circuit was drastically reduced by the gain of the transistor.

FIGURE 5. The cascade control technique



To correct the transistor non-linear properties the Cascade Control technique is used as shown in figure 5.

The Cascade Control is used when a transducer responds poorly to the control signal or is non-linear. The slave control loop controls the transducer thus the input to the slave controller will activate the transducer in a linear manner. The master controller now supplies its required transducer setting to the slave controller. Cascade Control requires the slave loop to have far quicker response time than master loop.

Referring to figure 5, the slave loop is being used to set the current in the transistors using an op-amp to compare the control input of with the volt drop across a resistor in series with the heating transistors. Thus producing a linear relationship between control voltage and power input to the oven enclosure.

The temperature sensor an LM135 produces an almost linear output of 10mV/Degree Celsius. A thermistor would have required various components to produce a linear output while the LM135 requires only a current limiting resistor to produce a linear voltage output. The master controller is provided by op-amp which compares a precision reference diode with the temperature sensor passing the error voltage to slave loop controlling the heater transistors.

### CALCULATION OF THE OVEN TRANSFER FUNCTION

The temperature sensor was positioned close to one of the heater transistors to minimise the time delay between the transistor drawing current and the temperature change being sensed.

This delay was estimated to be 4 seconds and assumed to be a pure time delay. The oven was then heated to 45 degrees Celsius and allowed to cool from which the oven time constant of 1140 seconds was chosen. From the above measurements the Laplace transfer function for the oven could be approximated to.

$$G_p(s) = \frac{e^{-4s}}{1 + 1140s}$$

The above equation is a first order lag with pure time delay. This is not the full transfer function as ambient temperature changes have not been included, although ambient temperature changes can be ignored if they are assumed to be slowly changing.

### SYSTEM GAIN K

The overall gain of the system could be expressed as -

( sensor output ( Volts/degree Celsius ) \* master cont gain \* cascade controller conversion ratio of degrees Celsius out / Volts in ).

The cascade voltage conversion ratio was found by applying a voltage to the cascade controller input and then measuring the temperature change of the oven. This was calculated to be 6.41 degrees C / V. The only variable left which can be altered is the Master Controller Gain ( KMC ).

$$K = 10\text{mV} * \text{KMC} * 6.41 = 0.0641 * \text{KMC}$$

The master gain was increased until the control system became unstable .

This occurred at KMC of 5000 making  $K_u = 5000 * 0.0641 = 320.5$ .

The value of 320.5 if used would give a very unstable control system but gives an indication of how high the system gain can be increased before instability is reached.

The gain must therefore be reduced to allow a safety margin. This was investigated by Ziegler & Nichols in the 1940's ( Ref 2 ). They provided recommended values for various control systems. For this case of proportional control they recommend that the stable gain ( Kc ) should be set to half the gain at which system oscillates ( Ku ).

$$K_c = 0.5 K_u$$

$$K_c = 320.5 * 0.5 = 160.25$$

### CAD SIMULATION

Simulation of the control system using the CAD package CODAS was used to observe the behaviour of the system. The CODAS program requires the Laplace transform for the system and information such as limited control effort ( maximum transistor current )

CAD simulation confirmed that the temperature control system be stable and have a low steady state error. However it must be noted that the pure time delay is the limiting factor for both stability and steady state error of the control system. *Positioning of the temperature sensor is therefore a critical factor in determining the performance of the system.*

### MECHANICAL CONSTRUCTION

#### ANALOGUE CIRCUIT

To ensure good performance from the analogue electronics a double sided circuit board was used with the upper face being used as an ground plane. Using a ground plane not only reduces noise and pick-up between tracks, but in this application it was essential to avoid IR volt drops. With an 18 bit device over a 5v range the LSB = 0.000019V without a ground plane board the earthing arrangements would have caused problems.

The circuit board contained two DAC channels.

#### OVEN ENCLOSURE

A standard die-cast enclosure was used for the oven. The die-cast box was chosen because it provided shielding for the analogue circuit from electromagnetic interference and proved to be a good thermal conductor.

### THE NEED FOR CALIBRATION SOFTWARE

The calibration of the dual unit to its full specification requires the adjustment of 24 ten turn potentiometer and when the unit is commissioned, or if the DAC729KH is replaced, the selection of up to 48 resistors.

Sixteen of the above adjustments are gain and offset adjustments and are not difficult to adjust and check but the remaining eight ( four per channel ) correct the linearity of the DAC. IC several point measurements would be required to do this.

1. To make the DAC729KH linear to 18 bit requires correcting the weighting of the 4 most significant bits using the following procedure.

With bits 1 to 14 all switched on the output voltage is measured, and to this measured voltage the value of the least significant bit is now added.

Adding binary "1" to bit 1 to 14 on would switch bits 1 to 14 off and bit 15 on . So with bit 15 on and all others off the output voltage can be set to the above combination of bits 1 to  $14 + 1 \text{ LSB} = \text{bit } 15$ .

The above procedure is done for the following -

Adjust MSB-3 bits 1 to  $14 + 1 \text{ LSB} = \text{bit } 15$

Adjust MSB-2 bits 1 to  $15 + 1 \text{ LSB} = \text{bit } 16$

Adjust MSB-1 bits 1 to  $16 + 1 \text{ LSB} = \text{bit } 17$

Adjust MSB bits 1 to  $17 + 1 \text{ LSB} = \text{bit } 18$

Adjust offset

Adjust gain

Repeat the above until no adjustment is required.

The above adjustments are interrelated if the MSB -3 is set incorrectly the following 5 settings will be incorrect.

2. Checking the linearity involves the measurement of a number of points across the output span to see if they would plot to a straight line. This procedure is time consuming but must be done to check that the adjustments done in 1. are correct.

3. When the unit was completed attempts were made to calibrate it manually. This proved very time consuming and it was difficult to achieve better than a 16 bit linear output using the above method.

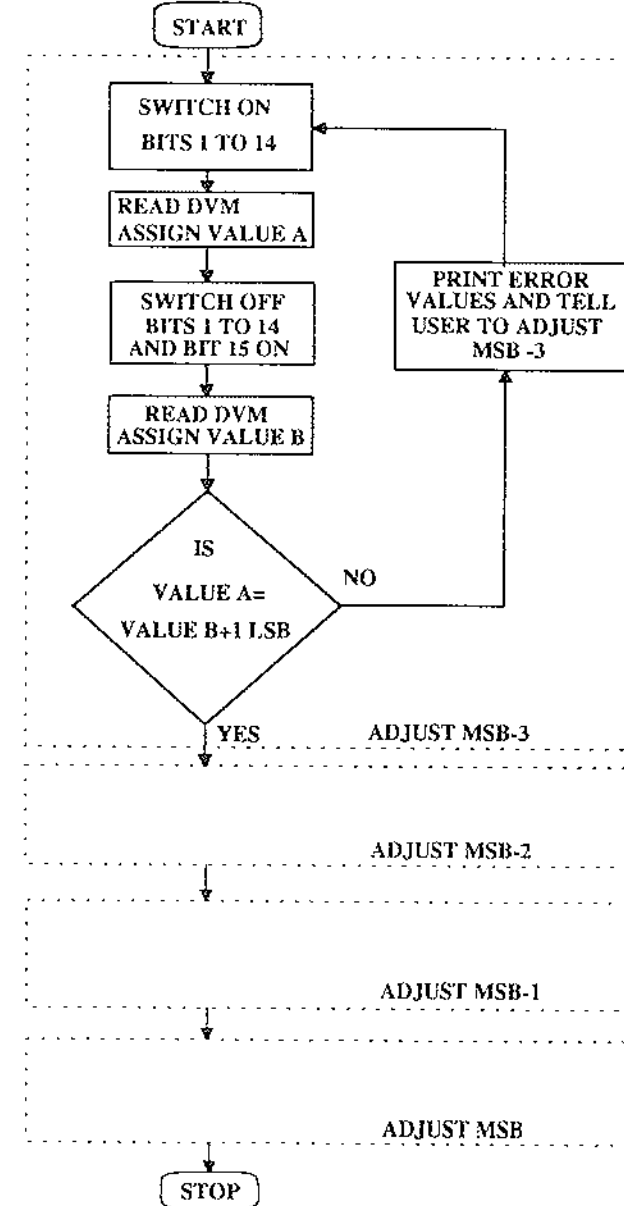
4. Correct calibration requires an in-depth knowledge of the operation of the DAC.

The above procedures are mainly repetitive calculations thus ideal for incorporation into software.

The program flow diagram is shown in figure 6.

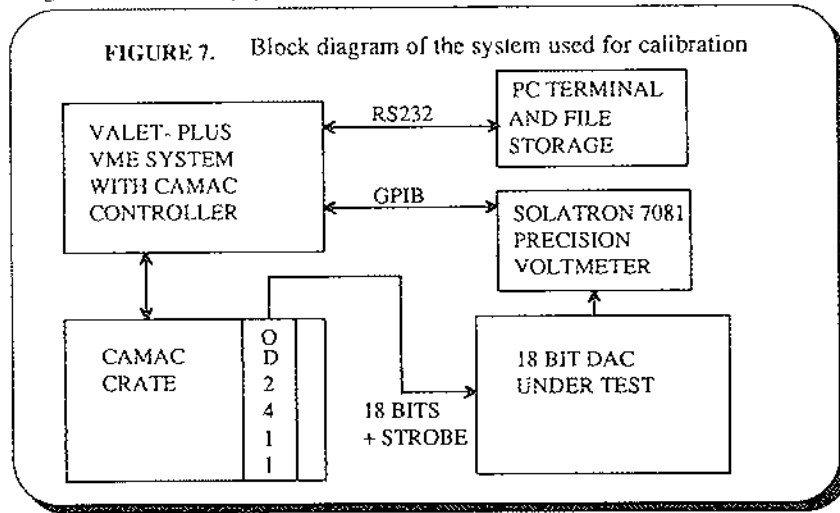
FIGURE 6.

LINEARITY ADJUSTMENT FLOW CHART



### SYSTEM USED FOR CALIBRATION

Figure 7. shows the equipment used to develop and use the calibration and test programs.



The system works as follows.

1. The PC is used as a terminal and to store program listing in text format
2. A MVME101 processor with ROM and RAM cards performs all the processing functions in the VME crate.
3. The VME crate is fitted with serial, GPIB and CAMAC interfaces which it uses to communicate in this case with the PC, DVM and DUAL DAC respectively.

The programming language used is PILS ( Ref 3). PILS is ideally suited to this application as it was supplied with subroutines for driving a GPIB interface which was used to read and control the DVM. PILS resembles the Basic language in structure.

### RESULTS

Several groups of measurements were taken on both channels of the unit constructed.

These results were obtained by placing the unit in an environmental oven whereby the ambient temperature under which the unit was operating was controllable.

The results are summarised in graphical form. Two separate measures of reference were obtained.

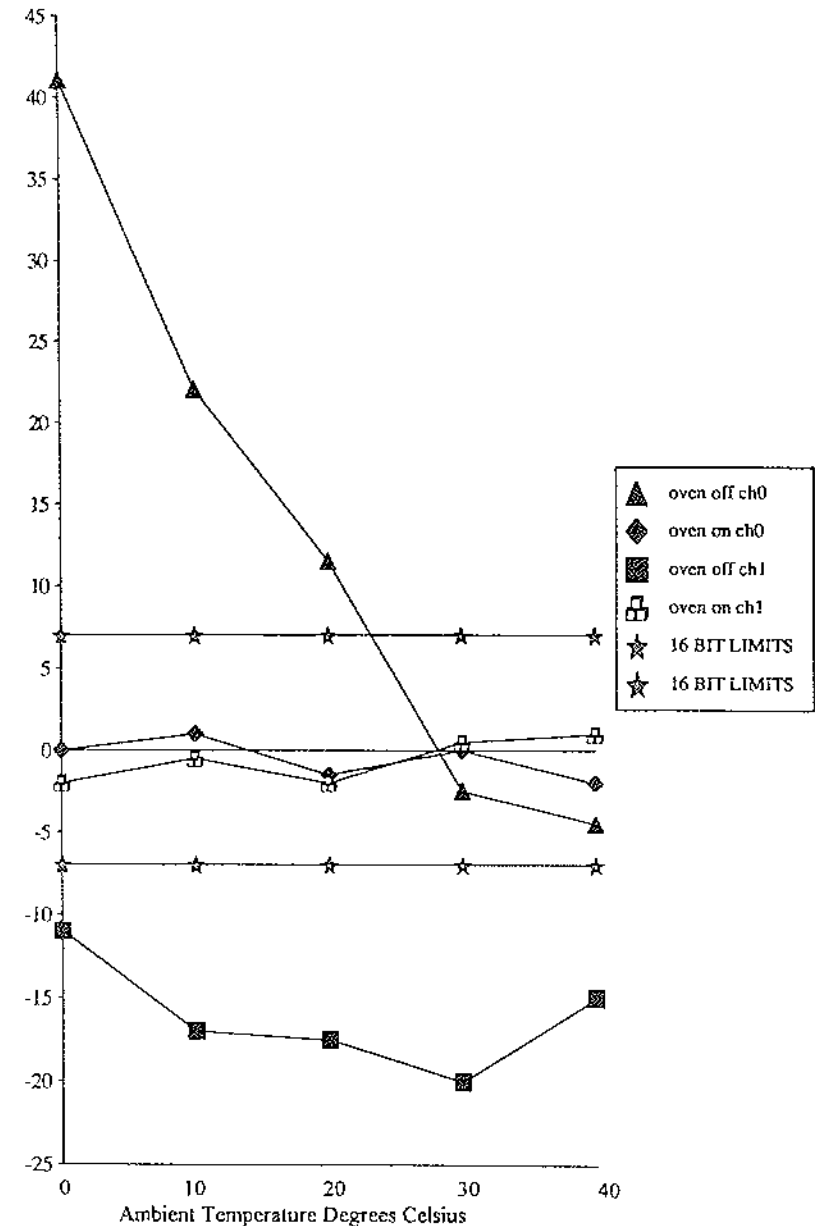
1. Reference Drift Figure 8. The DAC output was set to  $-10\text{v}$  on a  $+10\text{v}$  to  $-10\text{V}$  range, as the  $-10\text{v}$  offset is created from the DAC IC voltage reference this measurement shows any drift in the voltage reference, output buffer op-amp and offset adjustment potentiometers.

2. Gain Drift Figure 9. The DAC output was set to  $+10\text{v}$  on a  $+10\text{v}$  to  $-10\text{v}$  range. This measurement includes the drifts in (1) but also includes DAC IC resistor ladder and gain potentiometers.

**FIG 8**

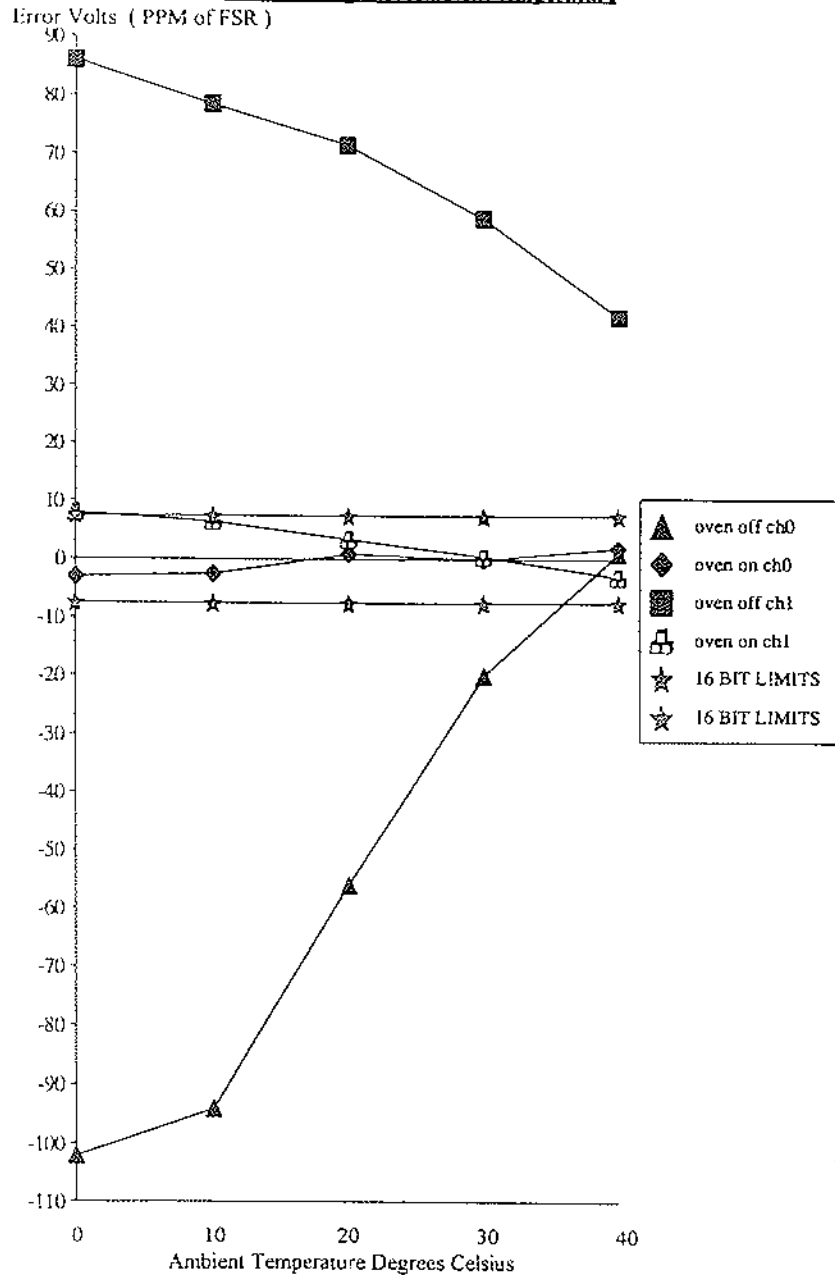
**Reference Drift against Ambient Temperature**

Error Volts ( PPM of FSR )



**FIGURE 2.**

**Gain Drift against Ambient temperature**



### CONCLUSIONS

To obtain truly accurate 16 bit DAC systems requires great care to minimise the effects of temperature drift. High stability components must be used in changing gain and offset.

To hold accuracy for repeatable measurements in anything other than laboratory conditions requires highly stable temperature control and is essential to obtain anything other than meaningless statements with regard to 16 bit systems.

### ACKNOWLEDGEMENTS

I would like to thank the following people-

Mr G.E.Derbyshire for introducing me to the field of data conversion and his help in writing this memorandum also Mr A.M.Cooper and Mr B.Straw "my line management and colleagues" for allowing the project to take place.

### REFERENCES

- 1) Burr Brown integrated circuits data book volume 33
- 2) Handbook of Automation Computation and Control Volume 3, Eugene M. Crabbe  
Simon Ramo  
Dean E. Wooldridge.
- 3) PILS Reference Manual Version 4, Robert D. Russell  
(C) CERN,CH-1211 Geneva 23 Louis Tremblet  
David O. Williams

This document may be printed via the CERN IBM VM/CMS documentation scheme CERND0C with the command: **DOCPRINT PILS MANUALS PILS (SGML**