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Beam Tests of a Prototype Level-1 Calorimeter Trigger for LHC Experiments

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Abstract

Beam tests of a first-prototype electromagnetic calorimeter trigger processor for LHC experiments are described. The synchronous, pipelined digital processor, built with ASICs, was successfully operated at the full LHC bunch-crossing frequency of 40 MHz. Real data signals were obtained from a liquid argon electromagnetic calorimeter. The measured performance of the electron/photon trigger algorithm is compared with Monte Carlo simulations.

1. Introduction

The Large Hadron Collider (LHC) [1] is the proposed proton–proton colliding beam machine to be built at CERN in the 27 km circumference LEP tunnel. The design centre-of-mass energy is $\sqrt{s}$ = 14 TeV with a luminosity of $L \approx 10^{34}$ cm^{-2}s^{-1}. Counter-rotating bunches of protons will cross in experimental areas at 25 ns intervals, corresponding to a rate of 40 MHz.

At $\sqrt{s}$ = 14 TeV the total proton–proton inelastic cross-section is ≈ 100 mb, corresponding to an interaction rate of $\approx 1 \times 10^9$ Hz at $L \approx 1 \times 10^{34}$ cm^{-2}s^{-1}. Hence, each bunch-crossing is expected to contain about 25 interactions. Most of these interactions do not involve any "hard" process and give rise only to low-transverse-momentum (low-p_T) particles. Only a tiny fraction of proton–proton interactions are expected to produce the "interesting" physics processes, such as production of Higgs bosons and their subsequent decays, that are sought at LHC.

Two collaborations, ATLAS [2] and CMS [3], are preparing proposals for general-purpose experiments for LHC. Both detector systems consist of inner tracking detectors, followed by electromagnetic and hadronic calorimeters, with external muon chambers. The detectors are highly granular because they must cope with the large particle multiplicity expected in each bunch crossing. High-performance trigger and data acquisition systems are essential parts of these experiments.

Multi-level trigger systems will be used to reduce the event rate from $\approx 1 \times 10^9$ interactions per second (4×10^7 bunch crossings per second) to ~ 10 – 100 Hz which can be recorded on permanent storage. The level-1 trigger will reduce the rate to ~ 10 – 100 kHz, a rate that is compatible with the front-end readout and microprocessor-based level-2 trigger systems. The level-1 latency should be as short as possible since the data for all detector elements must be stored in pipeline memories during this time; ATLAS and CMS aim for a latency of about 2 μs including signal collection, transmission delays to and from the trigger system, and the trigger processing time. During normal operation it is expected that the trigger will introduce negligible dead time. The level-1 trigger must uniquely identify the bunch-crossing containing the interaction of interest.

Signatures such as high-p_T muons, electrons and photons, jets, and large missing transverse energy indicate that interesting physics that we wish to study may have occurred. Additionally, such signatures allow discrimination against many background processes. With the exception of the muons, all of these signatures can be selected using calorimeter information in the level-1 trigger. As part of the RD27 project [4] we are studying algorithms and implementations for the level-1 calorimeter trigger.

Design studies for a complete level-1 calorimeter trigger system for an LHC experiment are well advanced [5], based on a synchronous, pipelined digital trigger processor. Such processors have been used successfully in collider experiments [6], although the LHC presents new challenges in terms of bunch-crossing rate, number of detector channels, detector occupancy and required rejection power. Purpose-built digital processors for the level-1 calorimeter trigger have many advantages over alternative technologies:

- It is possible to implement relatively complicated algorithms that optimise the trigger performance in terms of efficiency and rejection power. Many different sets of thresholds can be provided, and optional criteria such as electron/photon isolation can be implemented.

- A large degree of flexibility can be provided through programmable parameters such as thresholds and control words. Thus it should be possible to adapt the trigger to respond to new physics or unforeseen background conditions.
- Look-up tables can be employed for pedestal subtraction, calibration and applying geometrical factors.
- A programmable threshold can be applied at the trigger cell level, suppressing contributions from electronic noise and pile-up. The threshold can be increased for high-luminosity running (more pile-up) or in case of unforeseen problems such as coherent noise.
- Ease of calibration — the trigger ADC system can be cross-calibrated against the precision readout.
- Ease of monitoring — intermediate results from the calculation can be read out and checked against values calculated from the input data, requiring an exact match.
- Ease of testing and diagnostics — test patterns can be played through the processor, localising faults.
- The processing latency can be minimised using hardwired algorithms and fixed routing of the data by direct links.
- The interface between the digitisation system and the trigger processor can be optimised to cope with the extremely high bandwidth, for example by exploiting the low detector occupancy (zero suppression).
- It is relatively easy to equalise the phase of digital signals relative to one another, for example using programmable delays or FIFOs.
- Extensive use of Application Specific Integrated Circuits (ASICs) allows cost-effective implementations. Commercial CAD tools provide an easy route to a wide range of products from different vendors. Hence, one can exploit new technology as it becomes available and select among manufacturers to obtain the best price.

The electron/photon trigger is the most challenging part of the level-1 calorimeter trigger system. Relatively fine granularity is needed to obtain the required rejection power against the jet background (see below). A trigger-cell size of $\Delta\eta \times \Delta\varphi \approx 0.1 \times 0.1$ is typically used, where η is pseudo-rapidity and φ is azimuthal angle (radians), giving ≈ 4000 electromagnetic trigger cells for $|\eta| < 3$. Furthermore, complex two-dimensional cluster algorithms and isolation vetoes have to be used to separate isolated electrons from jets.

This paper describes beam tests of a first-prototype demonstrator digital calorimeter trigger processor, performing an electron/photon trigger using data from a 6×6 trigger-cell area of the RD3 "Accordion" liquid-argon calorimeter [7]. The input data were obtained by digitising analogue-summed signals from the calorimeter using 8-bit flash ADCs. The algorithm was performed in ASICs designed and produced for this project. The one-crate system was successfully operated at the full LHC bunch-crossing rate of 40 MHz.

2. Algorithm and Simulation Studies

An essential feature of the level-1 calorimeter trigger is to select isolated high-p_T electrons and photons with good efficiency while rejecting jets. Electrons and photons appear as localised clusters in the electromagnetic (EM) calorimeter, with little surrounding activity in the electromagnetic or the hadronic calorimeter. Typical transverse energy (E_T) thresholds

for this trigger are 40 GeV and 20 GeV for the single and two-cluster triggers respectively [2]. The algorithm must remain efficient in the presence of pile-up at high luminosity.

Jets can give rise to fake electron/photon triggers if they deposit sufficient energy in a local area of the EM calorimeter. This can happen if the jet contains one or more high-p_T π^0s, or because of early-showering hadrons. However, the resulting EM clusters tend to be accompanied by nearby energy deposits. Hence the background can be significantly reduced by means of an *isolation* requirement, although the level-1 trigger rate remains background-dominated.

Figure 1 shows our EM cluster algorithm, which operates on a 4 × 4 trigger-cell window. The transverse energies in 2 × 1 and 1 × 2 cells are computed and compared with the cluster threshold, giving good efficiency even if an electron/photon shower is not contained in a single cell. The E_T sum over the 12-cell ring in the EM calorimeter plus the 16-cell window in the hadron calorimeter is compared with the isolation threshold. The logic is duplicated for all possible window positions in the calorimeter, using a trigger cell size of $\Delta\eta \times \Delta\varphi \approx 0.1 \times 0.1$, with one depth sampling in each of the EM and hadronic calorimeters. Trigger cells with $E_T < 1$ GeV are not used in the algorithm so as to reduce the effects of electronic noise and pile-up.

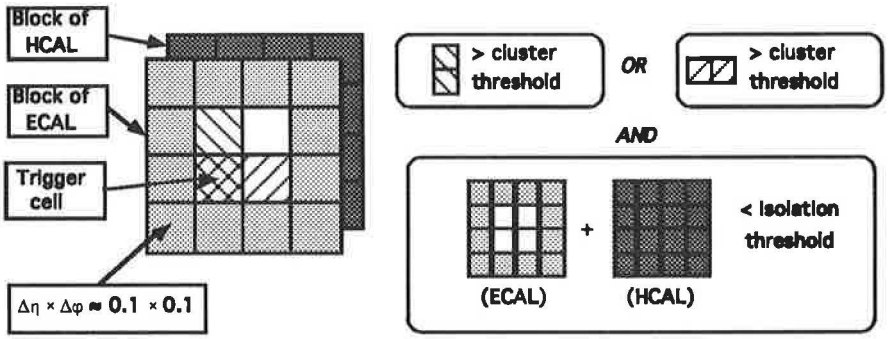

Figure 1: Schematic representation of the cluster algorithm.

The algorithm described above was chosen following extensive physics simulation studies. Efficiency studies were mainly made with single electrons, while jet events generated using Pythia [8] were used for background rate calculations. The trigger efficiencies for a variety of physics processes were also studied. The effect of pile-up was included in the efficiency calculations by superimposing an average of 20 minimum-bias events, generated with Pythia, on the signal events. (The simulations were performed for a luminosity $L = 1.7 \times 10^{34}$ $cm^{-2}s^{-1}$ and 15 ns bunch crossing which results in slightly lower pile-up). The detector simulation was performed using GEANT [9] with a slightly simplified model of the ATLAS detector [10] for the background studies, although a full version was used to study efficiency; the results are not strongly detector dependent. The simulation included the effects of electronic noise ($E_T = 0.36$ GeV per trigger-cell), digitisation (see below), gain variations between trigger-cells (5%) and fluctuations in the trigger ADC pedestals ($E_T = 0.2$ GeV per trigger-cell), as well as the calorimeter resolution ($\Delta E/E \approx 10\%/\sqrt{E}$).

The selected trigger cell granularity is a compromise between minimising the background rate due to jets, maximising the efficiency for electrons and photons taking into account the lateral spread of the EM showers, and having a system with a manageable and affordable number of trigger cells.

The simulation studies indicate that adequate performance can be achieved at level-1 using 8-bit linear ADCs with least count $E_T = 1$ GeV and full scale $E_T = 255$ GeV.

The high efficiency and sharp threshold behaviour of the algorithm are illustrated in Figure 2, which shows the trigger efficiency versus cluster threshold for simulated 50 GeV electrons. Also shown in the figure are the results for two alternative algorithms. Applying the cluster threshold to a single trigger cell results in a much less sharp threshold behaviour, while using a 2 × 2 cluster window is almost indistinguishable from the selected algorithm. A 2 × 2 window will almost fully contain all EM showers, and our algorithm loses little over this. Figure 3 shows the trigger rate (due to the jet background) versus cluster threshold for the three algorithms. Here the rate for the selected algorithm is significantly lower than with the 2 × 2 cluster window. Note that the results shown in Figure 2 are for $|\eta| \approx 0$ and that the inefficiency of the single cell algorithm, due to the sharing of EM showers between more than one trigger cell, becomes more marked in the forward regions, while the selected algorithm is less affected.

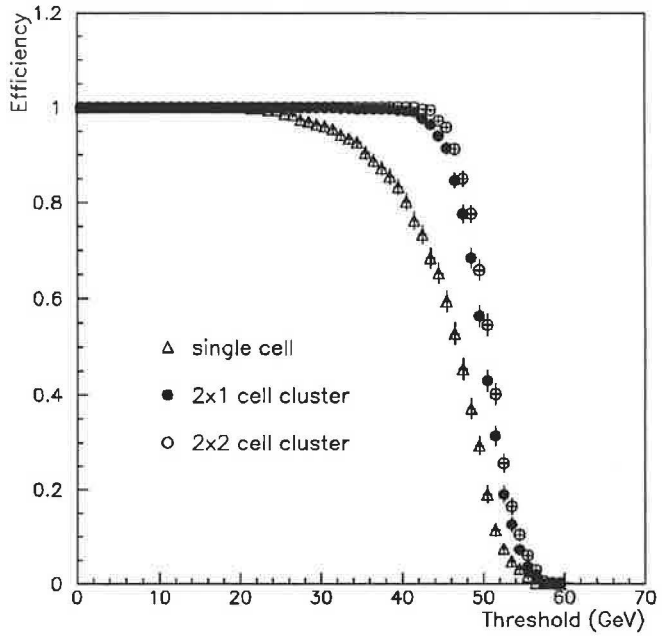

Figure 2: Efficiency versus nominal cluster threshold for 50 GeV electrons at $|\eta| \approx 0$.

Extra rejection against jet backgrounds can be obtained by using an isolation requirement. The effectiveness of isolation cuts is determined by the area of the isolation window, and by the tightness of the cuts that can be applied while retaining high efficiency for isolated EM showers. However, it is limited by electronic noise, pile-up and leakage of the EM shower itself into the isolation region. In the selected algorithm, the effects of electronic noise and pile-up are suppressed strongly by applying an E_T threshold to the individual trigger cells. However, this has the side-effect of somewhat reducing sensitivity to jet fragments with low p_T and hence the effectiveness of the isolation requirement. The trigger-cell threshold parameter (requiring $E_T > 1$ GeV) is crucial to the performance of the isolation veto.

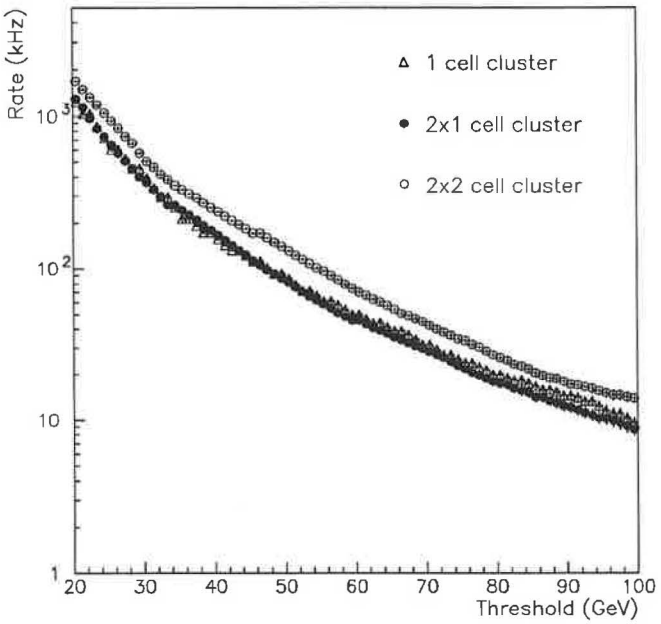

Figure 3: Trigger rate versus cluster threshold for $|\eta| < 2.5$ and luminosity 1.7×10^{34} cm^{-2}s^{-1}. The threshold value corresponds to 95% efficiency for electrons of the quoted energy.

The power of the isolation requirement is illustrated in Figure 4, which shows the background rate for the single-electron trigger versus cluster threshold, both without any isolation requirement and applying an isolation threshold of 5 GeV. With a typical cluster threshold of 40 GeV, the background rate is reduced by an order of magnitude to below 10 kHz, well within the capabilities of the level-2 trigger. The efficiency of the isolation requirement for isolated 50 GeV electrons, including the effect of pile-up at the highest LHC luminosity, is 97% as shown in Figure 5.

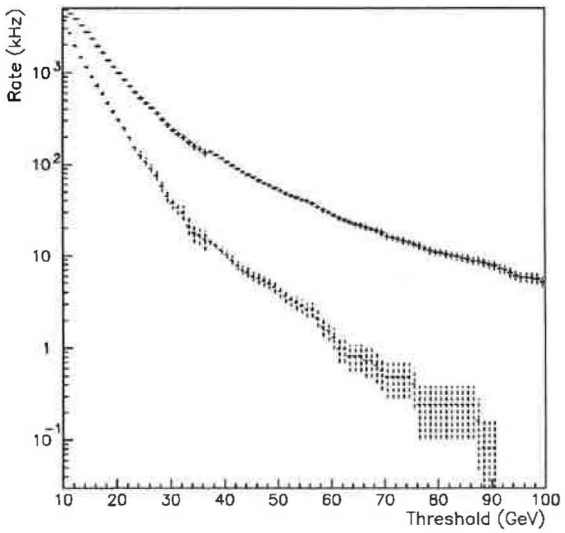

Figure 4: Trigger rate versus cluster threshold for $|\eta| < 2.5$ and luminosity 1.7×10^{34} cm^{-2}s^{-1}, with (lower curve) and without (upper curve) making the isolation requirement. The threshold value corresponds to 95% efficiency for electrons of the quoted energy.

It is worth noting that with the trigger-cell granularity of $\Delta\eta \times \Delta\varphi = 0.1 \times 0.1$ and a threshold of $E_T > 1$ GeV, the occupancy at $L \approx 10^{34}$ cm^{-2}s^{-1} is less than 10%. Design studies [5] that are in progress for a full level-1 calorimeter trigger system for an LHC experiment exploit this, using zero suppression to reduce the bandwidth required to send data to the trigger processor. This technique is being evaluated in the next phase of our R&D project.

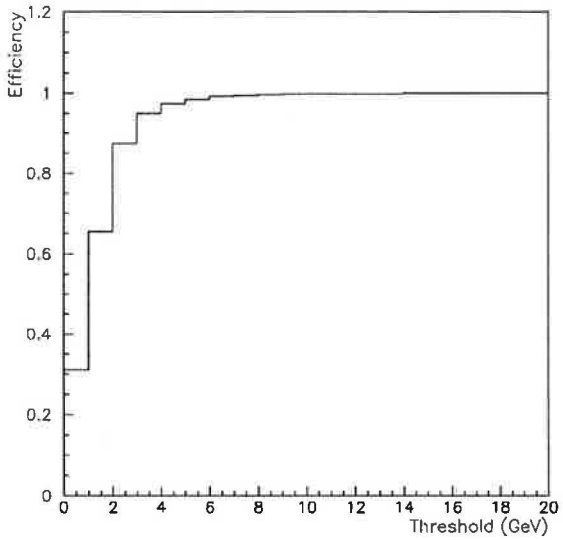

Figure 5: Efficiency for isolated electrons versus isolation threshold at $|\eta| \approx 0$. The calculation includes pile-up of an average of 20 minimum-bias events.

3. Demonstrator System

The algorithm described above has been implemented in an ASIC, which processes one trigger cell by taking in 8-bit data from an area of 4 × 4 EM calorimeter cells. One ASIC thus finds electromagnetic clusters centred on one reference trigger cell. In order to reduce the cost of the demonstrator system the information from the hadronic calorimeter is not included. Nine such ASICs have been incorporated in a demonstrator trigger processor module which services a 3 × 3 array and takes data from a 6 × 6 area of calorimeter trigger cells. The module also includes extensive test and monitoring facilities as described below.

A demonstrator calorimeter trigger system has been constructed including the processor and a system of flash ADCs (three 12-channel modules). The system has been tested extensively in the laboratory and in beam tests, where it was connected to the RD3 "Accordion" liquid-argon calorimeter [7] and operated in real time at the full LHC bunch-crossing rate of 40 MHz.

3.1 ASIC Implementation of the Algorithm

The cluster-finding ASIC [11] is a 0.8 μm CMOS gate array from Fujitsu (gate array type CG21203 – 20k), packaged as a 179-pin ceramic pin-grid array. Only about 6.4k gates are used to implement the algorithm, including two sets of cluster-threshold logic (e.g. for single-electron and two-electron triggers). During the design phase, a Verilog model was used for detailed behavioural simulation of the ASIC.

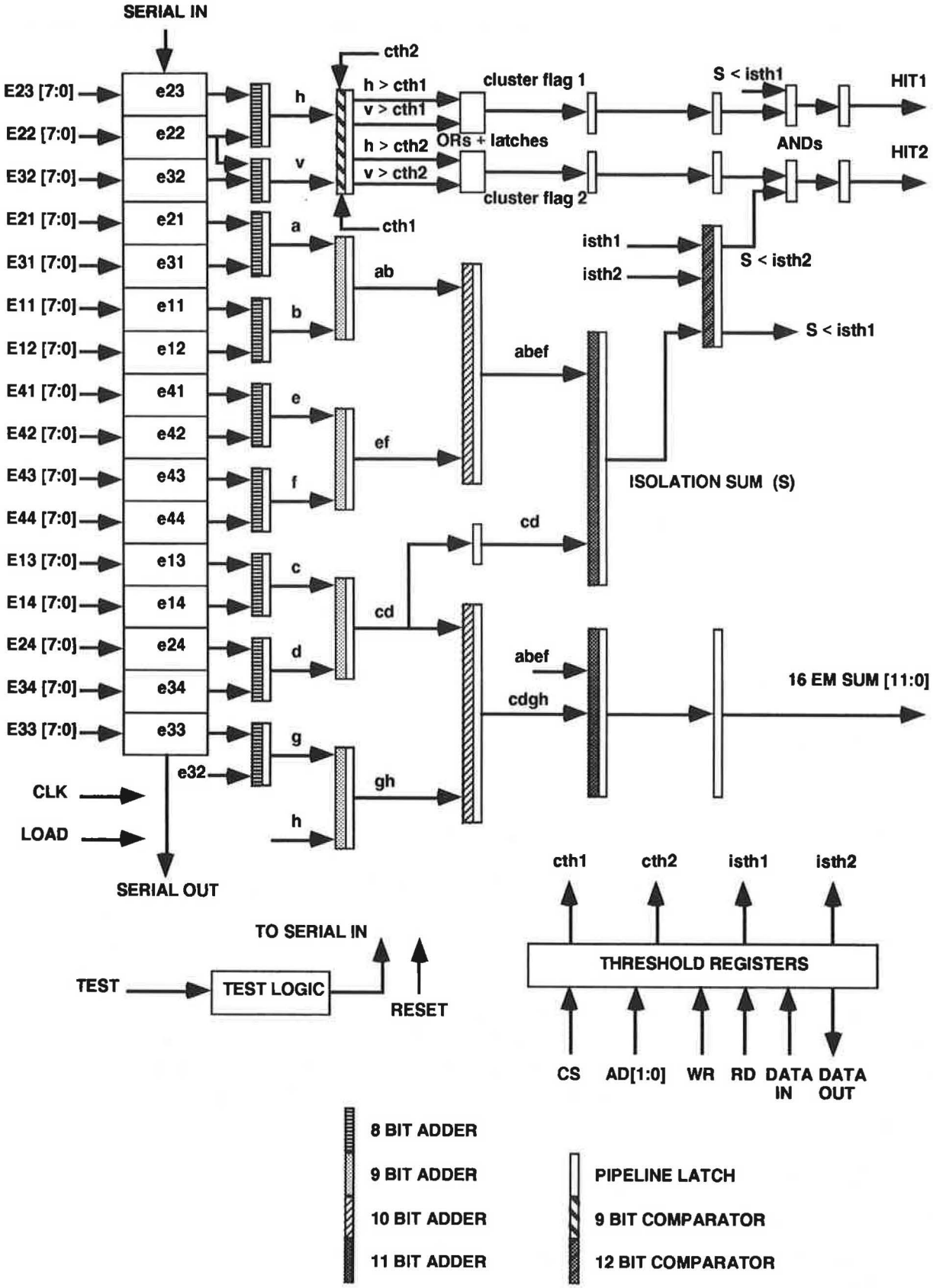

Figure 6: Block diagram of cluster-finding ASIC.

A block diagram of the ASIC logic is shown in Figure 6. The input data are sixteen 8-bit words giving the E_T in each of the trigger cells in the 4 × 4 window. The output data are two 1-bit "hit" flags (for the two sets of programmable threshold logic), plus a 12-bit transverse energy sum over the 16 trigger cells which could be used in subsequent jet and missing-E_T logic. The latencies are six and seven clock cycles for the energy sum and the hit flags respectively. Including slow control, test facilities and the clock, there are a total of 155 signal pins. The remaining pins are used for power (8 pins) and ground (16 pins).

The ASIC has been successfully tested in the laboratory at clock speeds up to 70 MHz, nearly twice the speed required for LHC assuming a 25 ns bunch-crossing period. The power dissipation of the device is 800 mW (at 67 MHz).

3.2 Demonstrator Module

The Cluster Finding Module (CFM) is a 9U high, 40 cm deep, 12 layer (8 signal, 4 power) printed circuit board which supports nine cluster-finding ASICs arranged in a 3 × 3 array. The fast input data from the ADC system arrive via the backplane (see below) as ECL signals. Following conversion to TTL levels, the data are fanned out to the different ASICs. The 36 × 8-bit input data are also stored in 256-deep circular buffers used for monitoring; these memories can also be used to feed test data into the processing ASICs. The hit outputs from the ASICs (9 × 2 hit bits) are transmitted to the front panel of the module as fast signals to be used in a real-time electron trigger; the energy sum from one of the nine ASICs is also available on the front panel. All the fast outputs from the ASICs (9 × 14 bits) are also stored in 256-deep FIFO memories used for monitoring. A block diagram of the module is shown in Figure 7.

The CFM has a very high density of components, partly due to the extensive test and monitoring facilities. SIMMs (Single In-line Memory Modules) were used for the input memories. A significant fraction of the board space is occupied by ECL/TTL level converters.

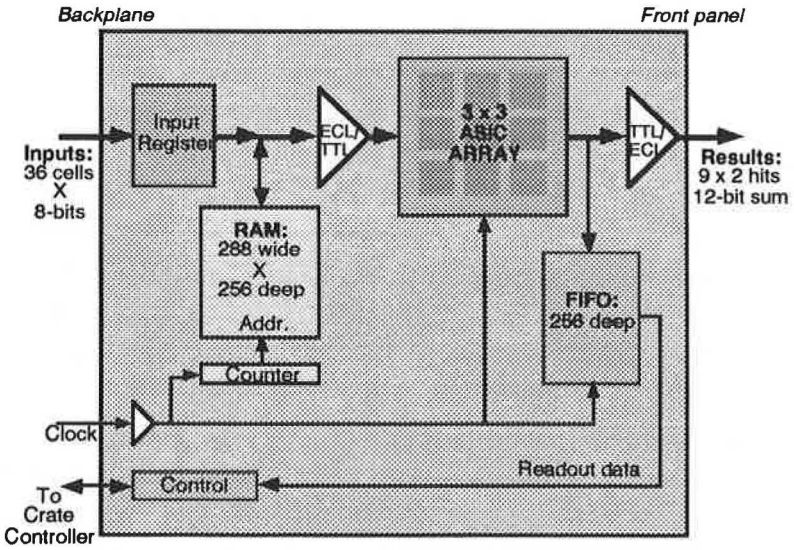

Figure 7: Block diagram of cluster-finding module.

The CFM has been successfully tested in the laboratory at clock speeds up to 70 MHz. At such speeds the board layout is critical and fine-tuning of clock phases on the board was required.

3.3 Demonstrator Crate

The demonstrator system crate supports 9U high, 40 cm deep modules. The bottom third of the crate backplane contains a standard bus used for slow control and readout, which is interfaced to VME. The upper two thirds of the crate have a purpose-built, wire-wrap backplane used for fast connections between trigger modules. High-density Teradyne connectors, with 320 active pins and 80 grounds, are used for the upper backplane.

The demonstrator system crate holds three ADC modules and the CFM. It also contains a clock module which provides correctly-phased clock signals to each of the ADC modules and the CFM. The bus between the ADCs and the CFM is terminated in a separate module, giving the possibility of distributing ADC data to more than one CFM.

Provision is made for Digital Signal Processing (DSP) modules which can be inserted between the ADCs and the CFM to perform bunch-crossing identification. The backplane connections are arranged so that, in the absence of DSP modules, the ADCs can occupy the "DSP slots" and drive the CFM directly.

Slow control and readout are performed via a crate-controller module previously used in the UA1 calorimeter trigger system [12].

The 12-channel ADC modules are based on flash ADC hybrid circuits designed for the Zeus drift-chamber readout [13]. The 8-bit ADCs (GEC SP97508) can be operated at speeds up to 110 MHz, although for most of the work described here a 40 MHz clock was used corresponding to the 25 ns LHC bunch-crossing period.

Additional modules which have been constructed are the following:

- A data-generator module used for laboratory tests of the system. This allows blocks of data, for example data previously recorded in beam tests, to be sent over the backplane into DSP modules or the CFM at the full 40 MHz rate. This is extremely valuable for testing and commissioning the system prior to beam tests. The data-generator module occupies either the ADC or the DSP slots in the crate.
- Interface modules that can be used to receive digital data from an external system. These have already been used in tests with the RD33 "TGT" calorimeter, for which a VME-based trigger ADC system is used[1].

4. Test Beam Set-up

The demonstrator trigger processor system has been used in joint tests with the RD3 "Accordion" liquid-argon calorimeter. The test-beam configuration is shown schematically in Figure 8. The objective of these tests was to demonstrate the operation of the processor in real time and to evaluate the algorithm in a test-beam environment. The tests of the demonstrator trigger system described here were performed during April and May 1993[2].

The granularity of the EM calorimeter under test corresponded to $\Delta\eta \times \Delta\varphi \approx 0.025 \times 0.025$ with three samplings in depth. Trigger-cell sums were formed by analogue summation over an area of 4 × 4 calorimeter cells laterally and over the first two depth samplings corresponding to a total of 18 X_0. The first stage of summation (lateral sum of 2 × 2

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1 Tests with the TGT calorimeter will be reported elsewhere.

2 Preliminary data were collected in November 1992 using a F1001 Flash ADC system [14] borrowed from the H1 experiment. These data were subsequently used in laboratory tests of the trigger processor in playback mode and for studies of the trigger algorithm.

calorimeter cells) was performed inside the RD3 shaper modules; commercial NIM linear fan-in modules (LeCroy LRS 428F) were used to complete the analogue summing. The summed signals were then sent to the trigger ADC system over 40 m long coaxial cables.

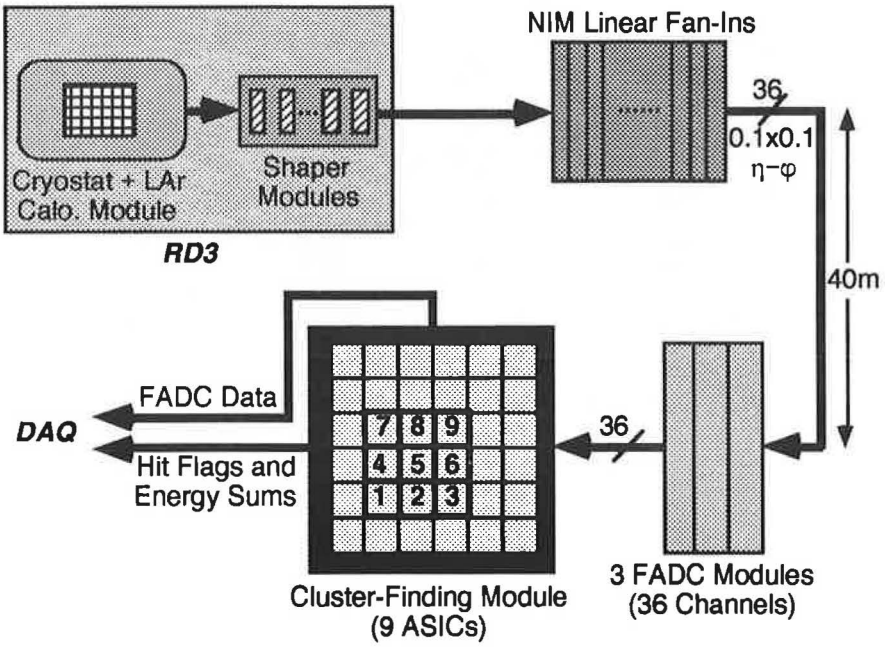

Figure 8: Block diagram of the calorimeter and trigger system.

The trigger processor and ADC system were operated using a free-running 40 MHz clock (some data were also recorded at higher clock speeds). At LHC, the clock will be synchronised with the bunch crossings and the phase of the ADC strobes will be adjusted to sample the calorimeter pulses at their maxima. This is not the case at the test beam, where beam particles arrive at random times. A CAMAC TDC was therefore used to record the phase of the clock relative to the arrival time of the beam particle. The sensitivity of the trigger ADCs in these tests was about 0.8 – 0.9 GeV per count.

Data from the trigger system were read out and recorded on Exabyte tapes using a VME-based data-acquisition (DAQ) system [15]. A beam trigger based on scintillator hodoscopes was used to initiate the readout, freezing the contents of the memories at the input and output of the CFM. Following each beam trigger, a time frame corresponding to between 20 and 248 samplings was read out from the trigger processor and recorded, allowing study of the time-history of the input and output data. The recorded data also include the TDC value, read out via a VME – CAMAC branch driver. This allowed detailed off-line evaluation of the trigger performance, as described below.

The RD27 DAQ system was interfaced to the RD3 DAQ system via a CES VIC link. A copy of the RD27 data was recorded on the RD3 data tapes along with the full-granularity calorimeter data. This allowed further tests of the trigger performance using the full EM and hadronic calorimeter data.

The prompt ECL front-panel outputs from the CFM were converted to NIM using a commercial level-converter module. Visual scalers were used to scale calorimeter processor triggers (OR of hit bits for one set of thresholds), beam triggers and the coincidence between the two. Figure 9 shows an oscilloscope photograph of a calorimeter pulse at the input to the trigger ADCs and the resulting trigger processor hit. The delay between the pulse and trigger is the sum of the processor latency, the time for the pulse to be digitised and cable delays, etc.

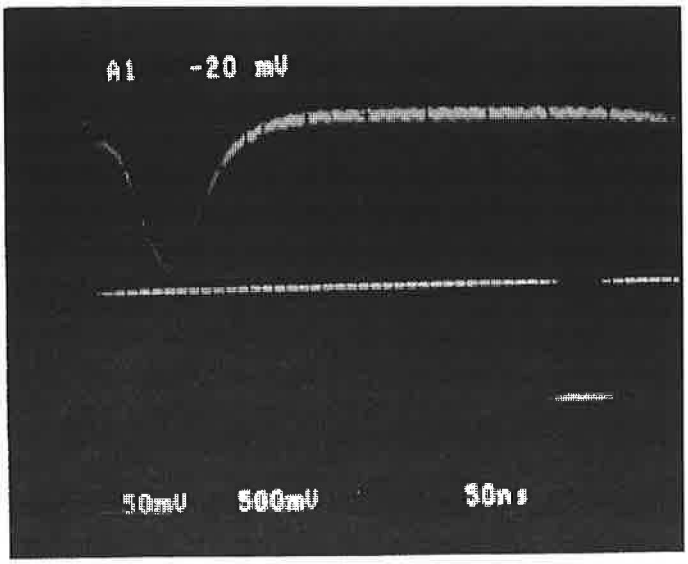

Figure 9: Oscilloscope photograph showing calorimeter signal at the input to the trigger ADC, and the trigger processor output.

Data were recorded with a wide variety of beam conditions, including pions and electrons of several beam energies. The thresholds loaded in the trigger processor were selected according to the beam energy. The data included a fine position scan with 50 GeV electrons at different positions within a single trigger cell.

5. Results

The trigger ADC data for each event record the pulse shape from each trigger channel, as illustrated in Figure 10 for a typical pulse. In this example the time frame was 60 clock cycles long with a clock period of 25 ns. The result of the bipolar shaping of the liquid-argon signal is clearly visible. The EM cluster algorithm sums the energy in horizontal and vertical pairs of trigger cells before applying a threshold, as illustrated in Figure 1. The resolution of the trigger with this cluster algorithm was determined using the TDC to select a subset of events in which the phase of the clock is such that the strobe to the ADCs is at the pulse maximum. The results[3] are shown in Table 1 for three representative beam energies; these results were obtained with the beam centred on the trigger cell. The resolution is dominated by pedestal fluctuations (typically 0.6 – 0.8 counts) and the coarse digitisation, and does not exhibit any energy dependence over the range of energies shown in the table.

Beam Energy	10 GeV	20 GeV	50 GeV
Measured rms	1.54 GeV	1.65 GeV	1.53 GeV
$10\%/\sqrt{E} \oplus 1\%$	0.33 GeV	0.49 GeV	0.87 GeV

Table 1: Measured and ideal energy resolution from the trigger ADC system. The bottom row corresponds approximately to the intrinsic resolution of the calorimeter without including electronic noise.

[3] Slightly better results were obtained using data from the November 1992 run, in which a different flash ADC system was used.

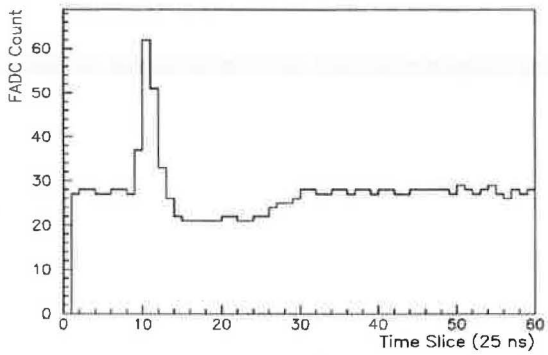

Figure 10: Accordion calorimeter pulse sampled by the trigger ADCs at 40 MHz.

To study the sharpness of the trigger threshold, electrons should be evenly distributed over the calorimeter surface. The beam spot was typically about the size of a calorimeter cell but the trigger cell had an area of 4 × 4 calorimeter cells. Therefore, in order to simulate the uniform distribution of electrons across trigger cells, data samples taken at different points within a trigger cell (in the centre, along the edges and in a corner) were combined. The plot of efficiency versus cluster threshold is shown in Figure 11a together with results of the Monte Carlo simulation. In these plots, the efficiency is obtained by taking the input flash ADC data and applying the EM cluster algorithm using software. In Figure 11b the corresponding plots are shown for an algorithm in which the threshold is applied to a single trigger cell rather than summing over horizontal and vertical pairs of cells; the single-cell algorithm exhibits a softer threshold behaviour. For both algorithms, the test-beam data are reasonably well reproduced by the Monte Carlo simulation.

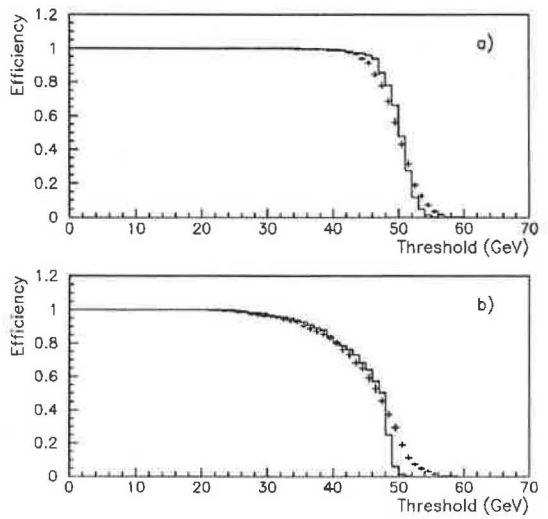

Figure 11: Trigger efficiency versus threshold for 50 GeV incident electrons. The solid histograms are the test-beam data and the points are a Monte Carlo simulation: (a) for two-cell algorithm, (b) for single-cell algorithm.

The other element of the EM cluster algorithm is the isolation requirement. This is primarily designed to reject jets mimicking the electron/photon signature, and thus the data taken during the beam tests with single particles incident tell us little about its performance. However, the efficiency of the requirement for isolated electrons and its dependence on noise

suppression can be studied. Figure 12 shows the efficiency versus the threshold on the energy measured in the EM isolation ring in events containing a 50 GeV electron cluster. This is shown for values of pedestal-subtracted cell threshold equal to zero and 2σ, where sigma is the rms deviation of the pedestal for the cell. Requiring that the pedestal-subtracted cell energy be greater than twice the pedestal rms is extremely effective in suppressing noise, and gives an efficiency of 95% for a requirement that the isolation energy be less than 5 GeV. The corresponding distribution from the Monte Carlo (MC) simulation is shown for comparison, assuming an rms noise level of 360 MeV per trigger cell.

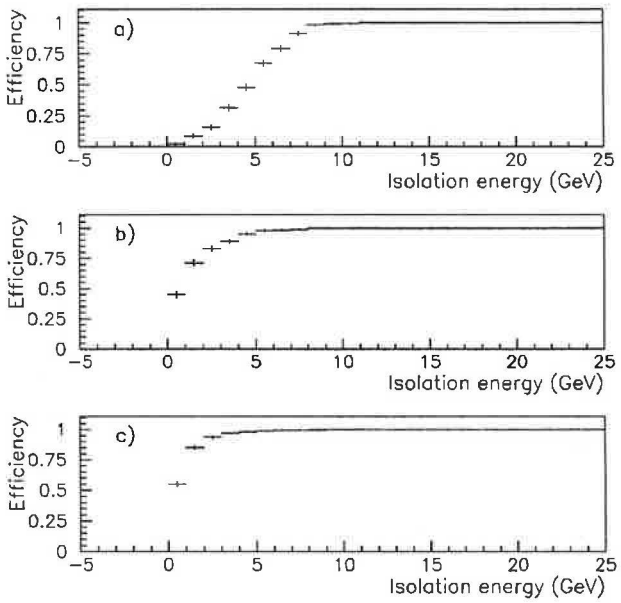

Figure 12: Trigger efficiency versus isolation threshold: (a) pedestal-subtracted data with cell threshold = 0, (b) pedestal-subtracted data with cell threshold = 2 σ, (c) MC simulation.

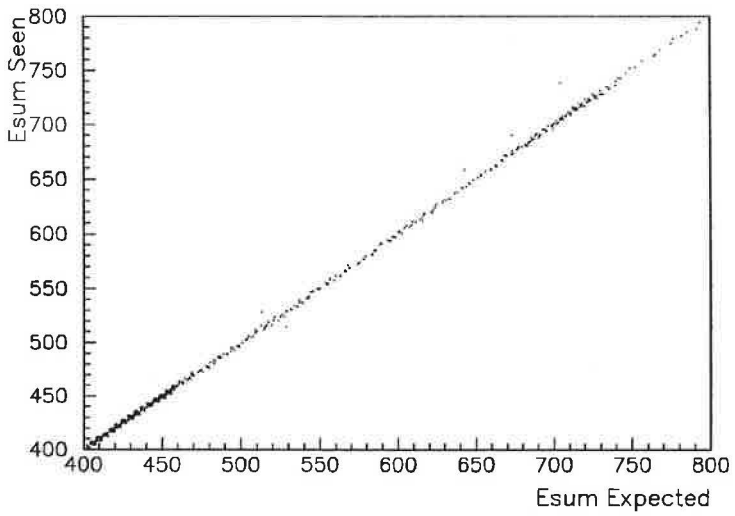

Figure 13: ASIC energy-sum output versus expected value after correcting for readout problem described in the text.

The real-time calculation of the 16-cell energy sum in the ASICs was checked by comparing the result read from the CFM output memories with the appropriate sum of ADC values recorded in the CFM input memories. After off-line correction for a minor error in the readout system (subsequently resolved in the real-time system), exact agreement was obtained in almost all cases. This is illustrated in Figure 13, which shows the energy sums calculated from the input ADC values versus the energy sums output from the CFM ASICs.

The reliability of the cluster threshold and the isolation threshold was also tested. Figure 14 shows the two-cell cluster sum for events in which a hit was or was not recorded. For this test the isolation requirement was disabled and the cluster threshold was set to 60 counts, close to the value obtained by summing the pedestals for two ADC channels. No spurious or missed triggers are observed. Figure 15 shows the 12-cell isolation sum for events in which a hit was or was not recorded. Here the isolation threshold was set to 360 counts, corresponding to 12 times the ADC pedestal value. Only events with a cluster above threshold were used so the test is purely of the isolation. Again no spurious or missed triggers are observed.

The results shown in Figures 13 – 15 indicate the successful operation of the CFM at the full frequency of the LHC, viz. 40 MHz.

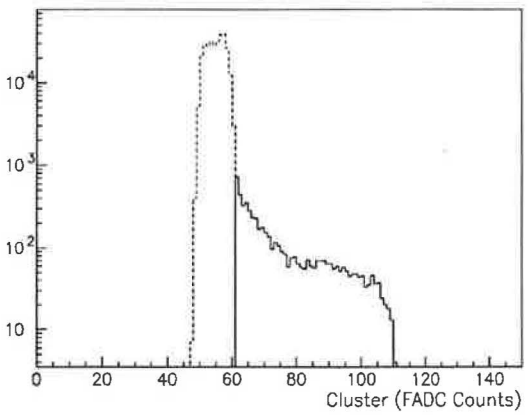

Figure 14: Energy in cluster window for events with (solid line) and without (dashed line) a trigger hit.

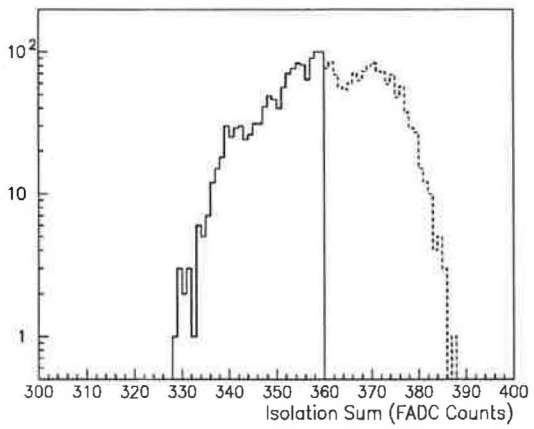

Figure 15: Energy in isolation ring for events with (solid line) and without (dashed line) a trigger hit.

The ability of the trigger processor to separate electrons from pions and muons in real time was demonstrated by analysing RD3 data tapes which included a copy of the RD27 data. Figure 16a shows a scatter plot of the total energies observed using the RD3 readout in the EM and in the hadronic calorimeters. Three distinct types of event can be seen — events with a large deposit of energy in the EM calorimeter and none in the hadronic calorimeter (electrons), events with little or no energy in either calorimeter (muons or spurious beam triggers), and events in which energy is shared between the two calorimeters (pions). Figure 16b shows the same distribution for events in which the EM cluster trigger fired, showing a sharp cut on the EM energy at about 150 GeV which eliminates the muons and a large fraction of the pions.

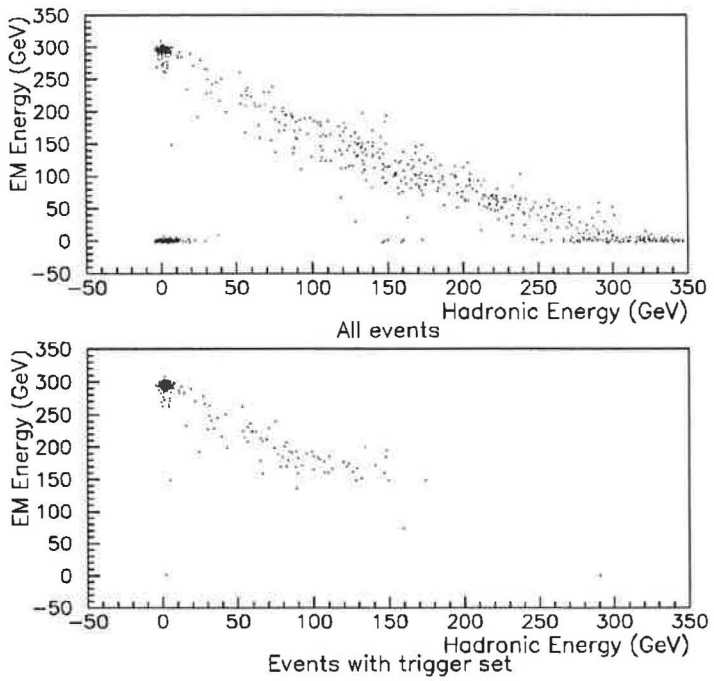

Figure 16: Total energy in EM calorimeter versus total energy in hadronic calorimeter: (a) for all events, (b) for events with an EM cluster trigger hit.

6. Conclusions

The level-1 calorimeter trigger will be an essential element of future LHC general-purpose experiments. An EM cluster algorithm for the electron/photon trigger, which includes an isolation requirement, has been chosen after extensive Monte Carlo simulation studies. The algorithm is efficient even in the presence of pile-up at the highest LHC luminosity, while having good rejection power against jets.

The EM cluster algorithm has been implemented in an ASIC and used in a first-prototype trigger demonstrator system. The electronics consist of a synchronous, pipelined, digital processor which includes many test and monitoring facilities. In the laboratory, the processor has been tested at above 70 MHz, well beyond the 40 MHz bunch-crossing frequency of LHC.

Extensive studies have also been made in a test-beam environment by connecting the demonstrator trigger processor to a liquid-argon calorimeter. The trigger processor was

operated at the full LHC frequency of 40 MHz. Analysis of the data show that the prototype processor worked reliably. The test-beam data are well reproduced by Monte Carlo predictions, giving an important check of the reliability of our simulations for LHC experiments. The ability of the processor to separate electrons from pions in real time was demonstrated.

The R&D on level-1 calorimeter trigger processors for LHC experiments is continuing and will be described in future publications. The ongoing programme of work includes the following:

- The study of digital filters for bunch-crossing identification, where a variety of algorithms are being evaluated and a demonstrator DSP module has been constructed and is under test. Initial results are available from the analysis of data collected with the RD3 liquid-argon calorimeter, for which the pulse duration is longer than 25 ns. These show that simple algorithms that can be implemented in a level-1 trigger system are capable of uniquely identifying the bunch crossing giving rise to calorimeter pulses.
- The design of a phase-2 demonstrator system, which will address the problem of connectivity between the digitisation system and the trigger processor. By using asynchronous serial transmission of zero-suppressed data at 160 Mbit/s, the number of input/output pins required will be reduced by a factor of eight compared to the first prototype.
- Design studies for a complete level-1 calorimeter trigger processor system for an LHC experiment. An outline design, using the EM cluster algorithm already evaluated in the phase-1 demonstrator and the data transmission scheme to be evaluated in the phase-2 demonstrator, already exists. In this design, the full level-1 calorimeter trigger processor will fit in six crates using technology that is already commercially available.

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